广东岭南职业技术学院
GUANGDONG LINGNAN
INSTITUTE OF TECHNOLOGY

校本教材——电子信息基础系列

电子信息专业英语
Protel 版

（第二版）

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内 容 简 介

本书为电子信息专业的专业英语教材。 Protel 99 是应用最广泛的电子线路设计软件，使用简单、易于学习、功能强大。本书以 Protel 99 英文版为基础，结合电子电路设计的特点，从实用角度出发，全面介绍了电路原理图的设计及印制电路板的设计方法。具体内容有 Prorel 99 基础、原理图设计环境的设置、电路原理图的设计、层次式原理图的设计、原理图元件的创建、电路板设计的基本知识、电路板设计环境设置、电路板规划和网络表的载入、印制电路板的设计、元件封装的创建、各种报表文件的生成及设计成果的输出，仿真等。全书内容翔实、层次分明、图文并茂、实例丰富，便于读者阅读和自学。本书面向高等院校电子信息类及相关专业学生，可作为电子信息专业英语教材，也可供电子线路设计工作者参考阅读。

第二版在先前版本的基础上，添加了词汇列表，以及实训环节的参考内容，供各位读者参考。

Contents

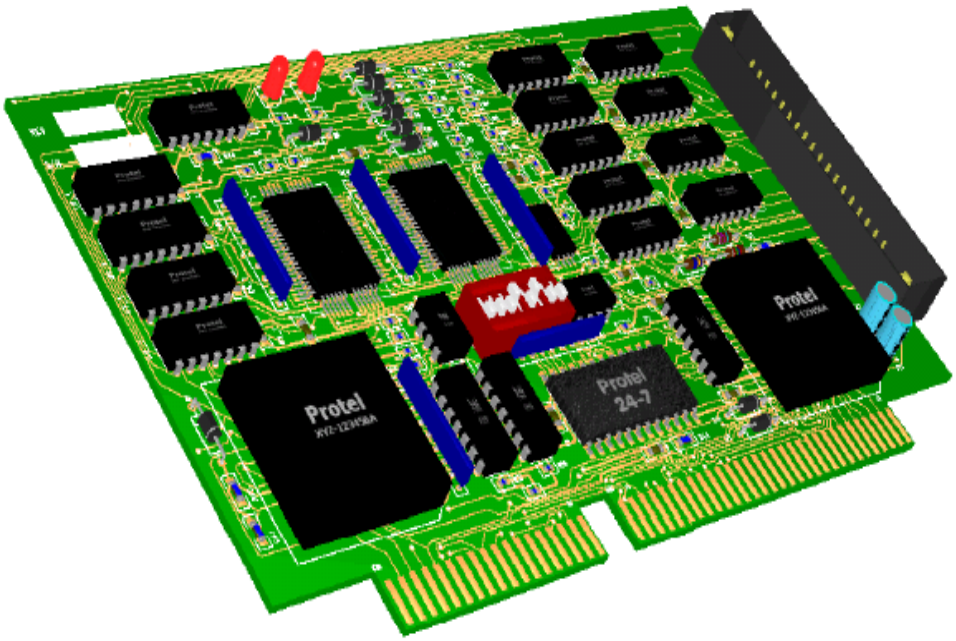
Unit 1 Increase your PCB Design Productivity With Protel 99 SE

Welcome to the Protel 99 SE Designer, your comprehensve guide to exploring and using the new and enhanced features included in Protel 99 SE. The information in this book will help you get the most from Protel 99 SE's advanced board design features, and complements the comprehensive information provided in this book.

Protel 99 SE is the version of Protel's integrated board-level design system for the Windows NT/98/95 operating system. It builds on the foundation of Protel's unique Design Explorer platform, introduced with the relrase of Protel 99, by adding a host of new and enhanced features aimed at streamlinng the board design process.

Protel 99 SE's Design Explorer integration platform has been optimized to give fast application and design document opening, more responsive performance and more efficient memory usage. You now have a choive of design data storage methods – save your integrated design in a single Access database, or as stand – alone files and folders using the simplicity of the Windows File System. With either storage method you have available the full power and convenience of Protel 99 SE's design

management and integration features.



From design entry through to manufacturing output creation, Protel 99 SE gives you greater design flexibility and power. Capture your design faster and more accurately with Protel 99 SE's enhanced schematic editor, that now features direct on-sheet text editing, sheet-by-sheet and positional annotation, automatic component class creation based on source schematic sheets, plus a host of time-saving editing and interface enhancements.

Create your board from 32 signal layers, 16 internal plane layers, and 16 mechanical layers, with fully-definable layer stackup and drill layer pairing. With enhanced power plane connectivity, new design rules and rule scopes, and import/export of design rule sets, Protel 99 SE's PCB editor gives you unparalleled versatility in board design definition.

New and enhanced interactive component placement tools will slash

design layout time. Protel 99 SE supports on-board graphical creation and editing of placement rooms, dynamic real-time optimization of connection lines during component moves, and the ability to group components for fast placement of component blocks.

New and enhanced interactive component placement tools will slash design layout time. Protel 99 SE supports on-board graphical creation and editing of placement rooms, dynamic real-time optimization of connection lines during component moves, and the ability to group components for fast placement of component blocks.

New PCB design features in Protel 99 SE include a powerful PCB print management system, an advanced 3D PCB renderer and viewer, and an invaluable CAM Manager that gives you “one click” output generation.

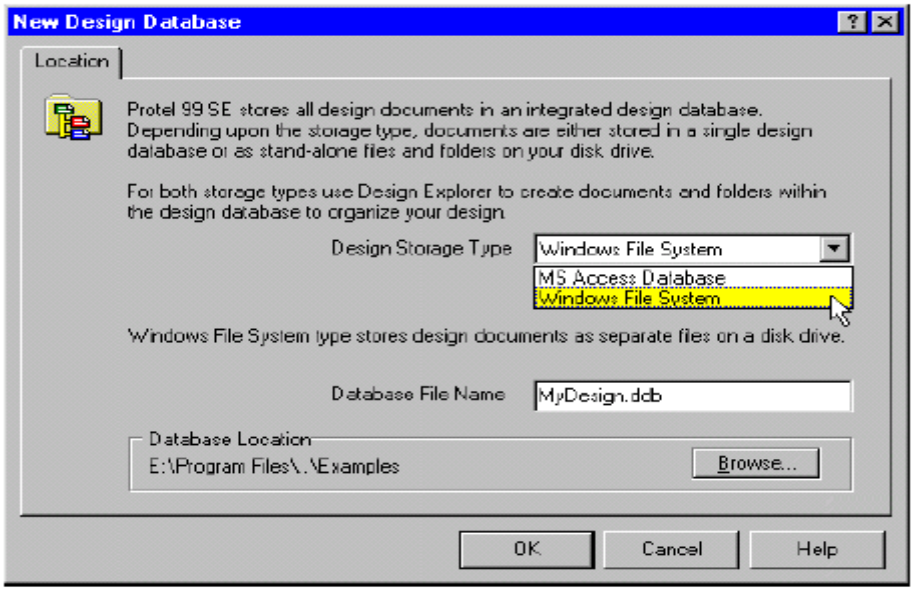
The above enhancements and features are just a taste of the many ways in which Protel 99 SE makes your desktop a more productive board design environment. Please explore this supplement and see just how much easier design can be with Protel 99 SE.

Unit 2 Design Explorer

The Design Explorer is the name given to the Protel 99 SE design environment. When you select Protel 99 from the Windows Start menu, the Design Explorer opens. The Design Explorer is the interface to your designs, and the various design tools that you use to create your designs.

Windows File System Storage Option

Protel 99 SE includes a new document storage option that stores design documents directly on a diskdrive. The New Design Database dialog includes a new Design Storage Type option, where you specify if the design documents will be stored in a single integrated Microsoft Access database, or if they will be stored directly on a disk drive.



Select the document storage type when you create a new design

If the Storage Type is set to MS Access Database then all design documents are stored in a single database. If the Storage Type is set to Windows File System then all design documents are stored directly on the disk drive in the location specified at the bottom of the dialog.

Regardless of the storage system that is chosen, the way you work in the Design Explorer is exactly the same. If your design uses the Windows File System Storage Type you still open the design first – then open the schematic, PCB, or other design documents.

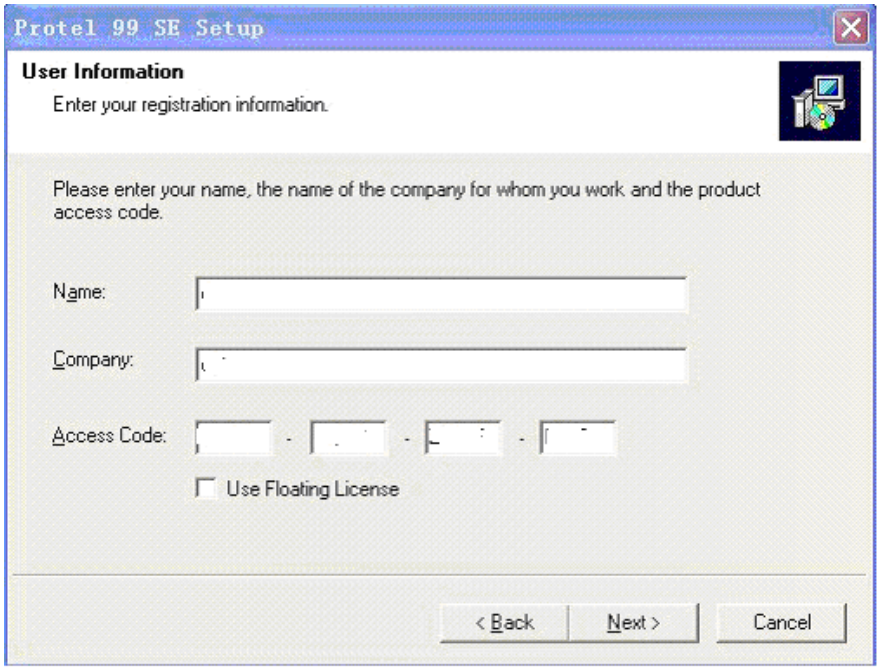
New documents are created in the same way for both storage types, select *File » New* to create a new document. Note that you can not move documents into a Windows File System database with the Windows File Explorer, they must be imported into a database before they can be opened. You can import a number of files by importing a folder, or by dragging from the Windows File Explorer directly into an open design.

Designs that use the Windows File System storage do not support any of the DesignTeam features, such as document access control. Other design integration features, like synchronization and background document opening when printing and netlisting, are supported.

Floating Licenses

Protel 99 SE supports floating licenses. This system allows you to install Protel 99 SE on as many PCs as you like – Protel 99 SE automatically monitors how many copies are running and displays a warning message when there are too many copies running at the same time.

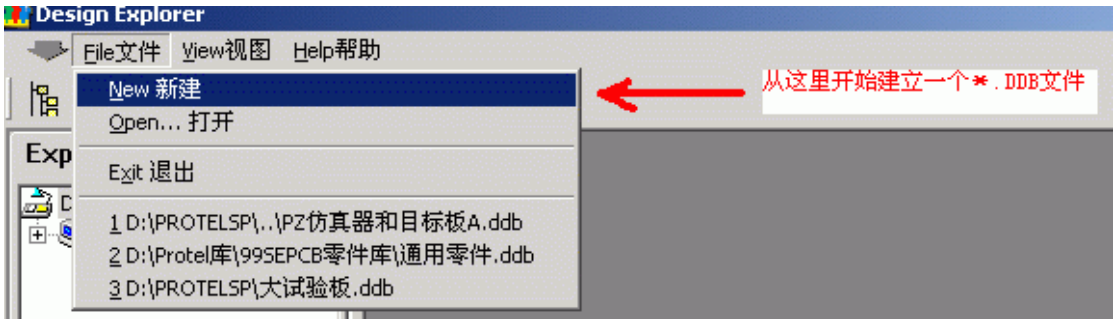
If your network includes PCs that must have a single-user license permanently allocated disable the Broadcast and Receive Floating Access Codes options at the bottom Security Locks dialog.


Protel 99 SE Setup
User Information
Enter your registration information.
Please enter your name, the name of the company for whom you work and the product access code.
Name:
Company:
Access Code:
Use Floating License
< Back
Next >
Cancel

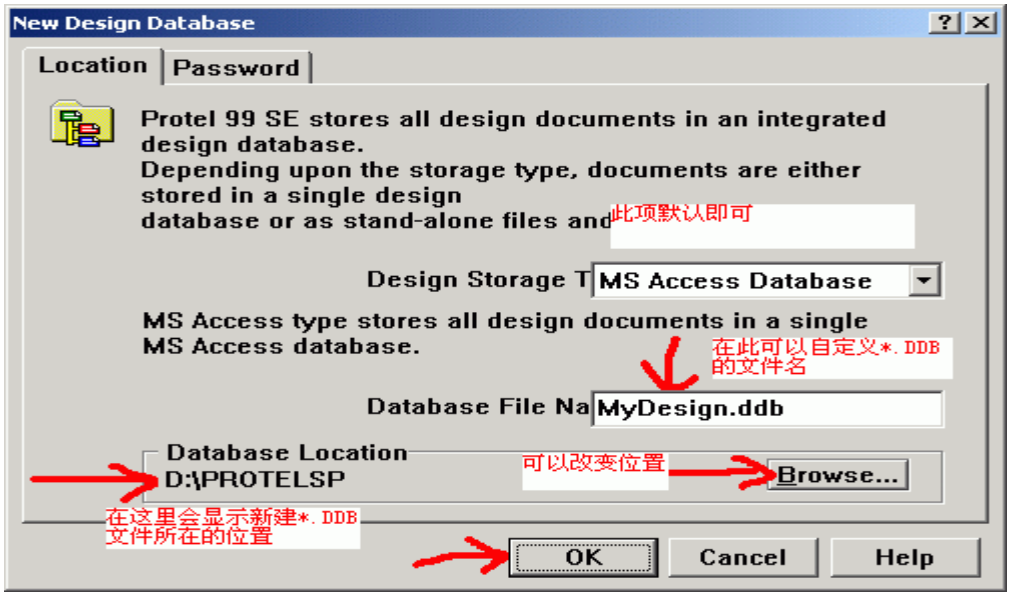
Unit 3 How to Start

Creating a new design

To create a new Design Database select File ?New Design from the menus. The New Design Database dialog will pop up. Complete the following steps:



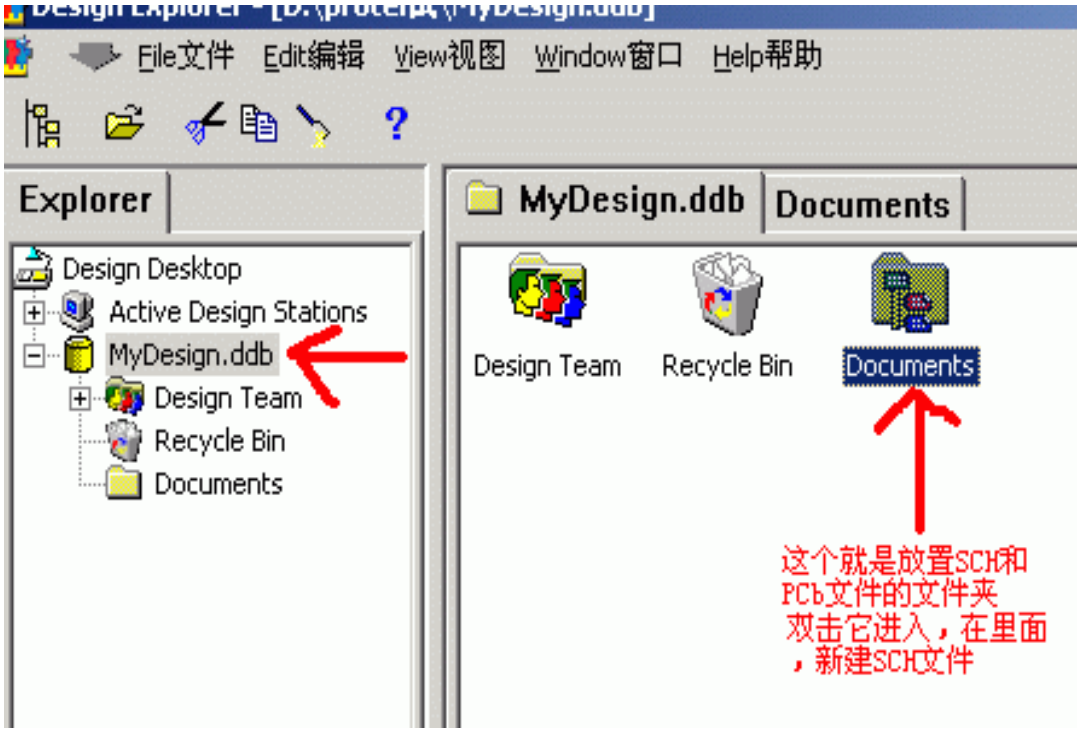
1. Select the Storage Type
2. Enter the Database name
3. Set the location as required



If you would like to password-protect the Design Database now, click on the Password tab and enter the password. This password is assigned to the default user name Admin. You can password-protect a Design Database at any time, by going to the Members folder and entering a password for the Admin member. To unprotect a Database remove the password from the Admin member. Note that you can only password-protect a design database whose storage type is MS Access database.

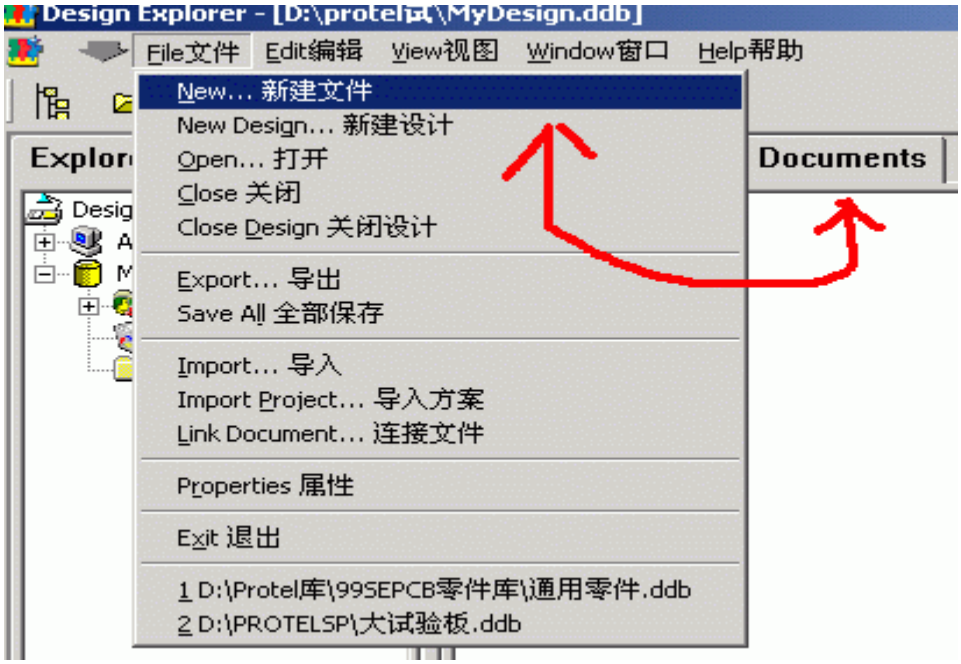
Once the new design database is created an icon for it will appear in the navigation tree of the Design Explorer, and its corresponding design window will open in the work area.

Then you will see the following picture:

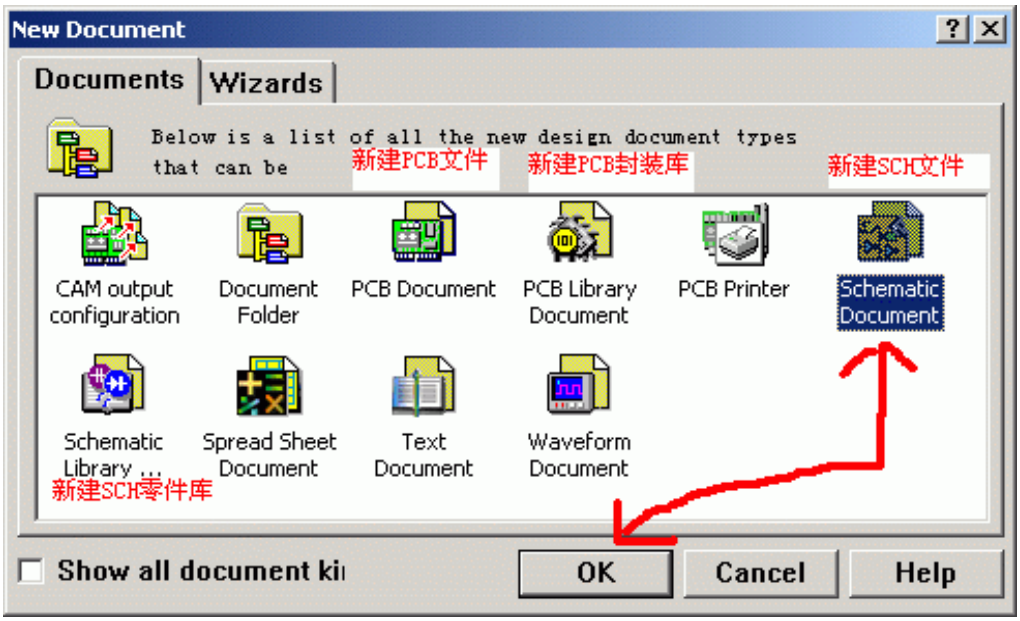


Adding a .SCH file

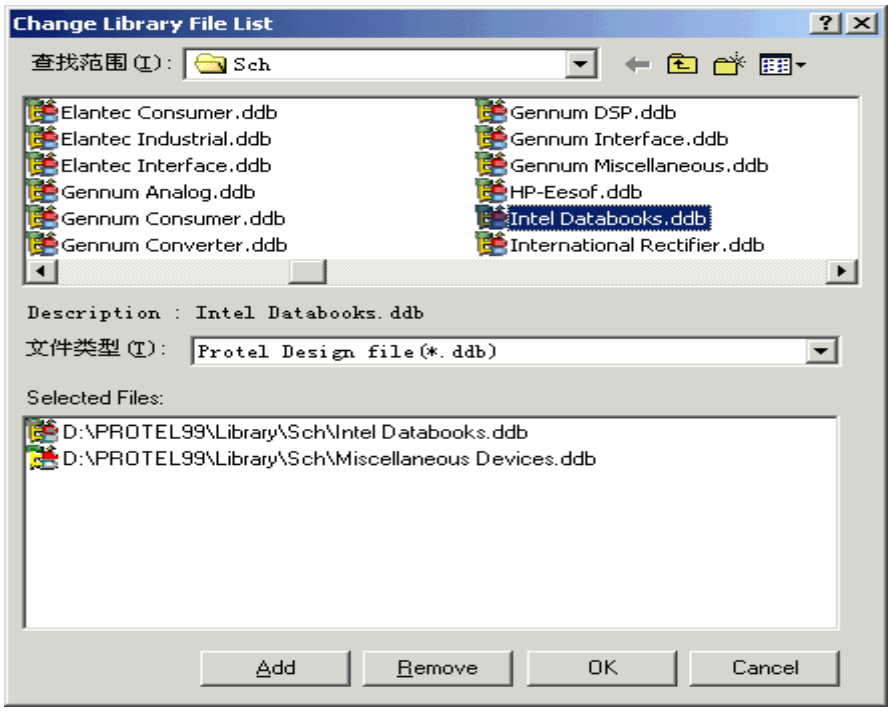
The first step is:



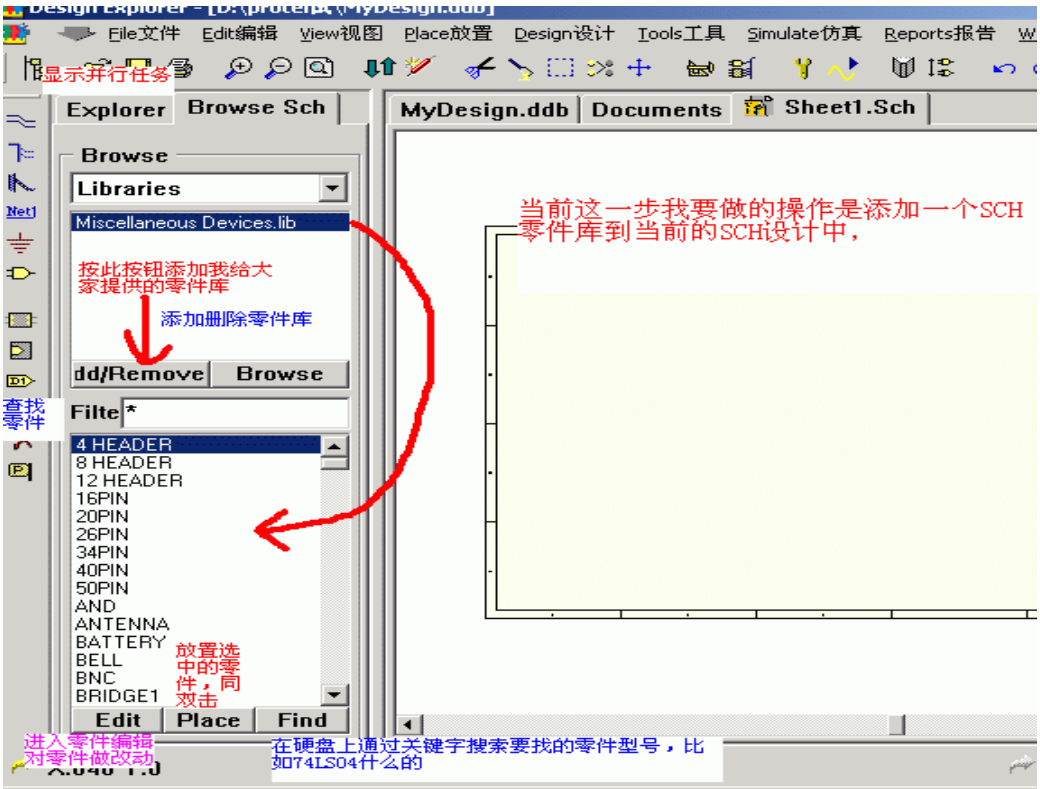
The second step is selecting the Schematic Document file:



The third step ,click the tab of the Browse Sch, you will see the following picture.



Select the design database(.ddb) files which you want, then click the Add button to add other design databases to the list. You can then browse within the design database that is currently selected. When you locate the required document click on it to select it, then click on the OK button.



Working with the Navigation Tree

The Design Explorer Design Manager panel provides a navigation tree with a Windows Explorer-like navigation panel that shows a hierarchical view of the documents and folders contained within an open design database. Folders are shown as folder icons in the tree, and documents are marked with an appropriate icon. A small box next to a tree branch indicates that the document or folder contains other documents or folders.

Unit 4 Working with design objects

Design objects are the building blocks of both schematic and PCB documents. You construct schematic and PCB designs by placing and arranging design objects on a schematic sheet or PCB layout document. Everything you use to construct you design is a design object, including components, tracks, wires, text annotations, etc.

The following topics detail the manipulation of design objects in Protel, and apply to both schematic and PCB designs.

Placing design objects in documents

The method for placing objects is similar for both schematic and PCB documents. The basic placement steps are outlined below.

1. Select the object that you want to place ? You can do this by selecting an object from the Place menu or by clicking on one of buttons from the various placement toolbars. For components and footprints, you can also click the Place button in the Panel when browsing libraries.

2. When an object is selected for placement, the cursor will change to a crosshair, indicating that you are in editing mode, and, if relevant, the

object will appear "floating" on the cursor.

3. Press the TAB key to edit the properties of the object before placing it. This will open the property dialog for the particular object, allowing you to change various options. Once you have finished setting the properties, close the dialog to return to placement mode.

4. Position the cursor and left-click or press ENTER to place the object. For complex objects such as wires, tracks, polygons, etc. you must continue the position and click procedure to place all vertices of the object. Note: If autopanning is active, you can move around the document by simply moving the cursor past the edge of the editing window in the direction that you wish to go.

5. After placing an object you will remain in placement mode (indicated by the crosshair cursor), allowing you to place another object of the same type immediately.

6. To end placement mode, right-click or press the ESC key (in some cases, such as placing a polygon, you may need to do this twice; once to finish placing the object and once to exit placement mode). When you exit placement mode, the cursor will return its default shape.

Editing design objects in documents

Any design objects you have placed in a schematic or PCB document

can be modified in a variety of ways. Objects can be moved around within the document, and cut, copied and pasted within and between documents. Also, you can edit the properties of objects to change their colors, layers, designator, net assignment, etc. With some objects, such as polyline shapes (tracks, wires, polygons, fills, etc), you can graphically change the shape of the object after it has been placed.

The topics below detail the general techniques for editing objects within PCB and schematic documents.

Changing the properties of a design object

All objects in schematic or PCB documents have a defined set of properties associated with them. These properties can include position, color, layer, selection status, etc. To view or edit the properties of any object, open its associated Properties dialog in one of the following ways:

1.When an object is "floating" on the cursor during the placement procedure, press the TAB key to open its properties dialog.

2.For any object placed in a document, double-click the object to open its properties dialog directly.

3.Select Edit → Change from the menus to enter the object change mode. Click on the object that you want to edit. Right-click or press ESC to exit object change mode.

Selecting design objects for editing

Before performing any editing action that operates on multiple design objects, such as aligning objects in schematic or PCB documents, you must first select the objects you wish to work with.

There are several ways to select objects:

1.Hold the SHIFT key down and left-click on an object.

2.Click-and-drag to draw a selection box around objects.

3.From a schematic or PCB document, select Edit ?Select from the menus to open the Selection submenu [shortcut S]. Use the item on this menu to make group selections in a number of ways.

Selected objects are outlined in the selection color (default is bright yellow). To change the default selection color, from a schematic or PCB document select Tools ?Preferences from the menus.

In Protel, selection of objects is cumulative: selected objects remain selected until you manually deselect them. Selecting additional objects DOES NOT deselect any objects currently selected.

To deselect an object:

1.Hold the SHIFT key down and left-click on a selected object.

2.From a schematic or PCB document, select Edit ?DeSelect from the menus to open the Deselection submenu [shortcut X]. Use the item on this menu to deselect groups of selected objects in a number of ways.

Setting the match attributes for global editing

When performing a global edit on an object type, the Attributes to Match By fields in the global editing portion of the object's properties dialog define the set of objects that the global edit will apply to.

If the property is a text field, you can use the "?" and "*" wildcard symbols to define the text in this field to match by. A ? defines any single character, and a * defines any group of characters. For example, to match all schematic components with designators of the form U1, U2, etc., you would enter the string U* in the Designator Attributes to Match By field.

Non-text fields will include a dropdown list in their corresponding Attributes to Match By fields, from which you can select Any, Same or Different to match objects which have any value, the same value or a different value respectively in these fields.

To define the set of objects you wish to apply the global edit to, set the appropriate Attributes to Match By fields to define the matching criteria. These fields are logically "ANDed" together to form the match criteria.

Unit 5 Working in schematic documents

Part 1 Schematic electrical design objects

A schematic is a diagrammatic representation of an electronic circuit, and schematic capture is the process of capturing a design as a schematic in a computer-aided design environment. A computer-based schematic is more than a simple drawing of the circuit. It also contains information about the connectivity of the circuit and the parts that make up the circuit.

In Protel, the basic workspace for capturing a schematic is called a schematic sheet. Electrical, drawing and directive objects are placed on a schematic sheet to design the circuit and produce working schematic drawings. A complete circuit design can use just a single sheet, or it can comprise a number of electrically linked sheets. Protel allows you to create complex hierarchical and modular designs by linking any number of sheets to form a complete project.

Schematic electrical design objects define the physical circuit you are capturing. These objects are used to create a netlist from the schematic, which is then used to transfer circuit and connection information between

design tools.

Bus (Schematic electrical design object)

Toolbar: WiringTools 

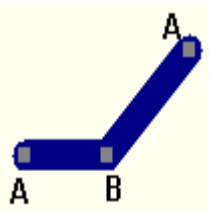
→  or Menu: Place →Bus

Description: A bus is a polyline object that represents a multi-wire connection. A bus can be assigned to multiple nets using a Net Label of the form "D[0..7]" or "D[7..0]", indicating that the nets D0 to D7 are carried by the bus. Use a Bus Entry object to connect to, or branch from a bus.

To place: Once in bus placement mode, left-click or press ENTER to anchor the starting point for the bus, then position the mouse and left-click or press ENTER to anchor a series of vertex points that define the shape of the bus. When you have finished drawing the bus, right-click or press ESC. Repeat the previous steps to draw another bus object, or right-click or press ESC to exit bus placement mode.

Press the TAB key during placement to edit the object's properties.

Graphical editing: When a bus object is in focus, the following editing handles are available. Click handles A to reposition the end points of the bus. Click handle B to move a bus vertex. The end points will remain anchored.Click near the center of a bus segment to grab that segment and reposition it.



Bus entry (Schematic electrical design object)

Toolbar: WiringTools  → 

or Menu: Place →Bus entry

Use a bus entry to connect to or branch from a bus object. Place the bus entry so that it touches the target bus object. The bus entry then forms a "stub" that you can use as a signal wiring point.

Part (Schematic electrical design object)

Toolbar: WiringTools  →  or Menu: Place →Part

A part is a schematic symbol that represents an electronic device, such as a resistor, switch, opamp, IC, etc. Parts are stored within components in schematic component libraries. A component within a library represents a physical device. Each component contains one or more parts.

Junction (Schematic electrical design object)

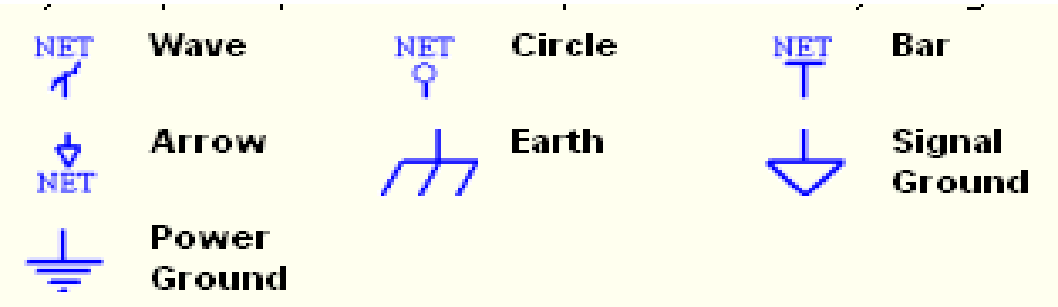
Toolbar: WiringTools  →  or Menu: Place →Junction

A junction forms an electrical connection where two or more wires cross. A junction is automatically inserted when a wire starts or terminates anywhere along the length of another wire. When a wire crosses other wires, no junction is inserted. If you want to create a connection between crossed wires, place a junction at the crossing point.

Power port (Schematic electrical design object)

WiringTools  →  or Menu: Place →Power port

A power port is a special schematic object that lets you easily define a power or ground net. Seven graphical styles of power port are available, and can be set by editing the object's properties.

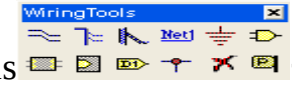


Wire (Schematic electrical design object)

WiringTools  →  or Menu: Place →Wire

A wire is a polyline object that forms an electrical connection between points on a schematic, and is analogous to a physical wire.

Net label (Schematic electrical design object)

WiringTools  →  or Menu: Place →Net label

A net label assigns a particular net name to an electrical object. When a netlist is generated, default names will be given to each net in the schematic. Manually placing a net label on your schematic defines the

name of the net to which it is attached.

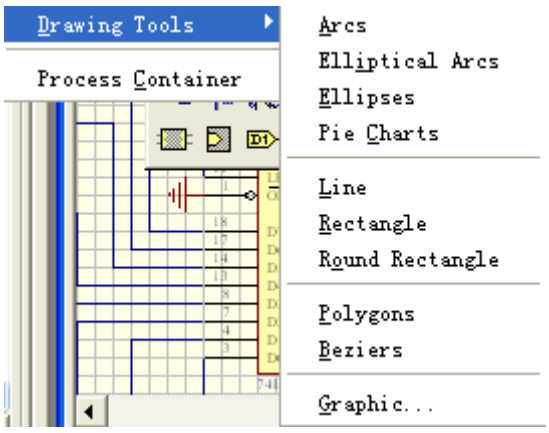
Port (Schematic electrical design object)

WiringTools 

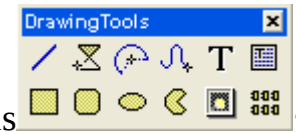
→  or Menu: Place →Port

A port is used to make an electrical connection between one schematic sheet and another sheet or sheet symbol in a design using multiple sheets. The name of the port, set in the port properties dialog (press TAB during placement, or double-click on a placed port to open this dialog), defines the connection (i.e. a port on a schematic sheet connects to ports or sheet entries with the same name on other sheets in the project).

Part 2 Schematic drawing objects



Annotation (Schematic drawing object)

Toolbar: DrawingTools 

→ 

Menu: Place→Annotation

Description:An annotation allows you to place a single line of free text on a schematic sheet. For more extensive, multi-line text, use the Text Frame object. Annotations are also used to reference special schematic information strings in schematic templates.

Text frame (Schematic drawing object)

Toolbar: DrawingTools 

→  Menu: Place→ Text Frame

Description: A text frame is used to define an area on a schematic to contain textual information. The frame is a resizable rectangular area that can contain multiple lines of text, and can automatically wrap text to keep it within the bounds of the frame. For simple one line text annotations, use the Annotation object.

Arc (Schematic drawing object)

Toolbar: none Menu: Place→Drawing Tools→Arcs

Description: Draws a circular arc on the current schematic sheet.

Elliptical arc (Schematic drawing object)

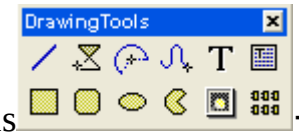
Toolbar: DrawingTools 

→ 

Menu: Place→Drawing Tools →Elliptical Arcs

Description: Draws an elliptical arc on the current schematic sheet

Ellipse (Schematic drawing object)

Toolbar: DrawingTools 

→ 

Menu: Place →Drawing Tools →Ellipses

Description: Draws an ellipse on the current schematic sheet.

Pie chart (Schematic drawing object)

Toolbar: DrawingTools 

→ 

Menu: Place→Drawing Tools→Pie Charts

Description: Draws a circular sector or "pie chart" object on the current schematic sheet.

Line (Schematic drawing object)

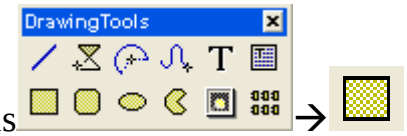
Toolbar: DrawingTools 

→ 

Menu: Place →Drawing Tools→Lines

Description: Draws a multi-segment line on the current schematic sheet.

Rectangle (Schematic drawing object)

Toolbar: DrawingTools 

Menu: Place→Drawing Tools→Rectangle

Description: Draws a rectangle on the current schematic sheet.

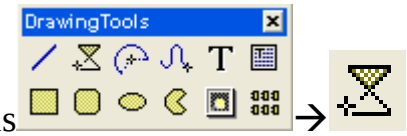
Round rectangle (Schematic drawing object)

Toolbar: DrawingTools 

Menu: Place →Drawing Tools →Round Rectangle

Description: Draws a rectangle with rounded corners on the current schematic sheet.

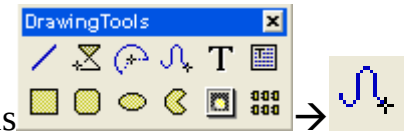
Polygon (Schematic drawing object)

Toolbar: DrawingTools 

Menu: Place →Drawing Tools →Polygons [P D P]

Description: Draws a polygon shape on the current schematic sheet.

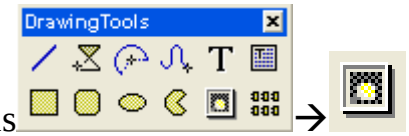
Bezier curve (Schematic drawing object)

Toolbar: DrawingTools 

Menu: Place →Drawing Tools →Beziers

Description: A Bezier curve allows you to draw free-form curved lines on a schematic sheet. The curve is defined by a series of vertex points that "pull" the line into a curved shape.

Graphic (Schematic drawing object)

Toolbar: DrawingTools 

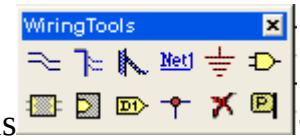
Menu: Place →Drawing Tools →Graphic

Description: This inserts a graphic file as an object in the current schematic sheet. The following file types are supported:1.Bitmaps (.bmp, .dib, .rle). 2.JPEGs (.jpg). 3.Windows Metafiles (.wmf)

Part 3 Schematic design directives

Schematic design directives attach additional design information to particular circuit nets. This information is not used in the schematic, but is incorporated into the netlist and can be used by other design tools, such as the autorouter or simulation engine.

No ERC (Schematic design directive)

Toolbar: WiringTools 

→ 

Menu: Place →Directives→No ERC

Description: Placing this directive on a node in the circuit suppresses any report warnings and Error Markers that may be generated for the node when running an Electrical Rules Check (ERC). Use this directive to deliberately prevent ERC checking of certain parts of a circuit that you know will generate a warning (such as unfinished connections) while checking the rest of the circuit.

Probe (Schematic design directive)

Toolbar: none

Menu: Place →Directives→Probe

Description: A Probe is a special marker which is placed on the worksheet to identify nodes for digital simulation during netlist generation.

Test vector index (Schematic design directive)

Toolbar: none

Menu: Place →Directives→Test Vector Index

Description: Test Vectors are special symbols used to identify a node with a simulation test vector. The test vectors are referred to by a column number, which indicates the column of the test vector file to use when the simulation is run. Note: This directive is currently not used internally by Protel.

Stimulus (Schematic design directive)

Toolbar: none

Menu: Place →Directives→Stimulus

Description: A Stimulus is a special symbol which is used to identify a node or net to be stimulated when the digital simulation is run.

PCB layout (Schematic design directive)

Toolbar: none

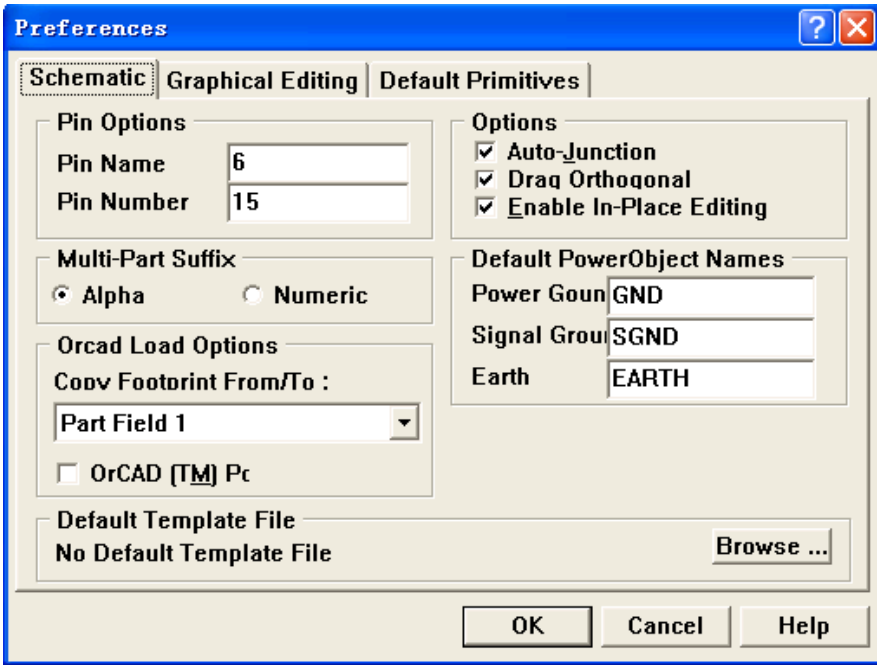
Menu: Place→Directives→PCB Layout

Description: Allows you to assign PCB layout information to a net in the schematic. When a PCB is created from the schematic, the information in the PCB Layout directive is used to create relevant PCB design rules.

Part 5　Setting schematic workspace preferences

Schematic preferences affect the schematic editing environment and are save as part of the Protel environment. These preferences apply to all schematic sheets.

To set the schematic environment preferences you must have a schematic sheet as the active document. Select Tools→Preferences from the menu to open the Preferences dialog. This dialog has three tabs:



Schematic tab:In this tab you control the appearance of the labeling of part pins, enable the Drag Orthogonal and Auto-Junctioning options, and set the default template used when creating new schematic documents.

Graphical Editing tab: In this tab you set various options controlling the editing environment, autopanning and undo/redo stack.

Default Primitives tab: In this tab you control the default properties and behavior of the design objects used to create schematics.

To set the default template used to create new schematic sheets, select Tools→Preferences from the menu when a schematic sheet is active. In the resulting Preferences dialog, make the Schematic tab active. In the Default Template File field, enter the path and name of a valid schematic template (schematic template files have a .DOT extension), or press the Browse button to search for a file.

When you are performing an editing action in a schematic sheet, moving the cursor to the edge of the work window will automatically pan the sheet in the appropriate direction, allowing you to navigate the sheet without having to use the scroll bars.

To control the speed of autopanning, or to turn off autopanning completely, select Tools→Preferences from the menu when a schematic sheet is active. In the resulting Preferences dialog, make the Graphical Editing tab active. Set the Autopan Options fields to change the autopanning behavior.

1.Style: Sets the way the sheet is scrolled during autopanning. Select an option from the dropdown list. Choosing Autopan off disables autopanning.

2.Speed: Sets the panning speed. This is independent of sheet size and sheet contents. Hold the SHIFT key to autopan at a higher speed.

For help on setting individual controls in the Preferences dialog, use the "What's This" help available when the dialog is open.

The visible grid is used as an aid for visually aligning objects on a schematic.

To change the way the visible grid is drawn, select Tools→Preferences from the menu when a schematic sheet is active. In the resulting Preferences dialog, make the Graphical Editing tab active.

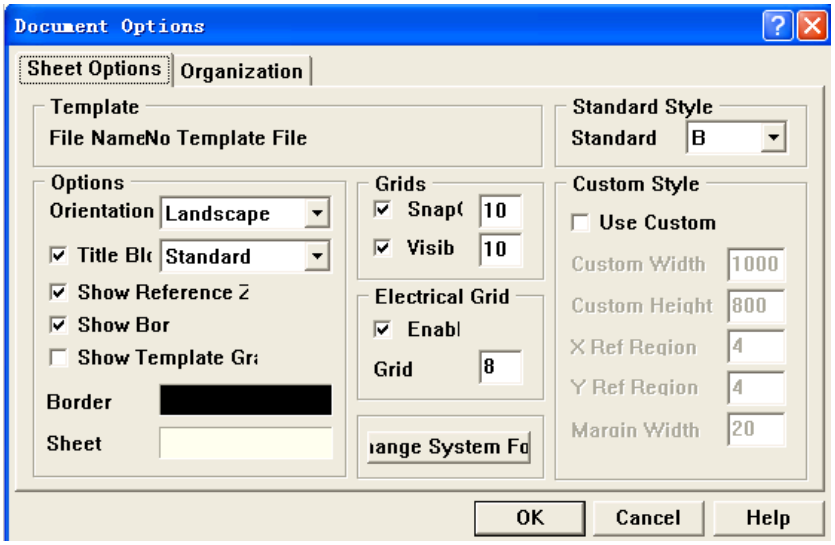
The lines used to draw the visible grid can be draw either solid or dotted. To select a line type, change the option in the Visible Grid field.

To set a color for the visible grid, click the color sample box in the Grid Color field and choose a color from the color selection dialog.

Part 6 Setting schematic document options

Schematic document options are properties of individual schematic sheets. These options are stored with the schematic sheet. Changing a document option only affects the currently active sheet.

To set the options for the active schematic sheet, select Design →Options from the menus to open the Document Options dialog. This dialog has two tabs:



Sheet Options tab: In this tab you configure the sheet size and orientation, border style, title block, grid ranges, background color, and system font.

1. To select a custom sheet size, enable the Use Custom Style option and set the desired values in the Custom Style fields.
2. Select the desired orientation in the Orientation field to set the schematic sheet orientation
3. You can automatically include a border and grid area around the edge of a schematic sheet. A border is a line around the edge of the drawing area. A grid area, or reference zone, draws a set of grid reference marks around the edge of the schematic inside the border area. To show or hide the border line, check or uncheck the Show Border option.To show or hide the reference zones, check or uncheck the Show Reference Zones option.
4. When performing any editing action in a schematic, the cursor movement is restricted to points that lie on the schematic snap

grid. This grid can be set independently from the visible grid. To enable or disable the snap grid, check or uncheck the SnapOn option. To set the size of the snap grid, enter a value in the SnapOn field.

5. The schematic electrical grid is a special grid designed to assist you in wiring up your schematic. The electrical grid defines a range around electrical objects within which the cursor is "captured" by the object, overriding the current snap grid. Wires, part pins, etc, are all affected by the electrical grid. With the electrical grid turned on, as you wire up your schematic, the cursor will automatically "find" electrical hot spots, making it easier to connect to electrical objects. To enable or disable the electrical grid, check or uncheck the Electrical Grid Enable option. To set the size or capture range of the electrical grid, enter a value in the Grid Range field.

6. The schematic visible grid is used purely as an aid for visually aligning objects on a schematic. The setting of this grid has no affect on the cursor movement during editing. To enable or disable the visible grid, check or uncheck the Visible option. To set the size of the snap grid, enter a value in the Visible field.

7. All text on a schematic sheet that is not part of a design object is rendered in the default font for that sheet. Items which use

this default font include: border text, system title blocks, pin names, pin numbers, ports, power ports and sheet entries. Press the Change System Font button on the to select a default font.

Organization tab: In this tab you enter company and design information to be used in the Title Block for the sheet.

Part 7 Using schematic sheet templates

he sheet border, title block and included graphics make up what is referred to as the sheet template. Protel 99 SE comes supplied with a number of sheet templates, one for each size of sheet available. Schematic templates are stored in the schematic Templates folder in the Templates.Ddb design database. This design database is in the \Design Explorer\System folder in the Protel installation directory on your hard disk.

To assign a template to a schematic sheet, from the schematic select Design →Template→Set Template File Name from the menus. The Select dialog will appear. The drop-down list at the top of the dialog includes all design databases that are currently open in the Design Explorer. To add the Templates.Ddb database click on the Add button, browse to the \Design Explorer\System folder and double click on the Templates.ddb file. You can now browse within this design database to the Schematic

Templates folder, and select the required template.

When you click OK the Set Template dialog will appear ,click OK to apply this template to just the active schematic, or Apply to All to update all schematics in this project. It will not affect other schematics in the design database that are not part of this project.

User defined sheet templates can be created. They are created in the same way you create a normal schematic sheet. After adding all the objects to the sheet that you want to appear in the template, select File→Save Copy As from the menus. In the resulting dialog, set the Format to either Schematic template binary or Schematic template ascii. You must give the template a name ending with a .DOT extension. Click OK to save the template file in the design database.

As well as including custom title blocks and graphics, sheet templates can include special strings to automatically add document text when printing or plotting.

Part 8 Managing schematic components

Schematic component descriptions are stored in schematic libraries, which can be stored within a design database or as external files named with a .LIB extension. The default schematic libraries supplied with Protel 99 SE are stored within a series of design databases located in the

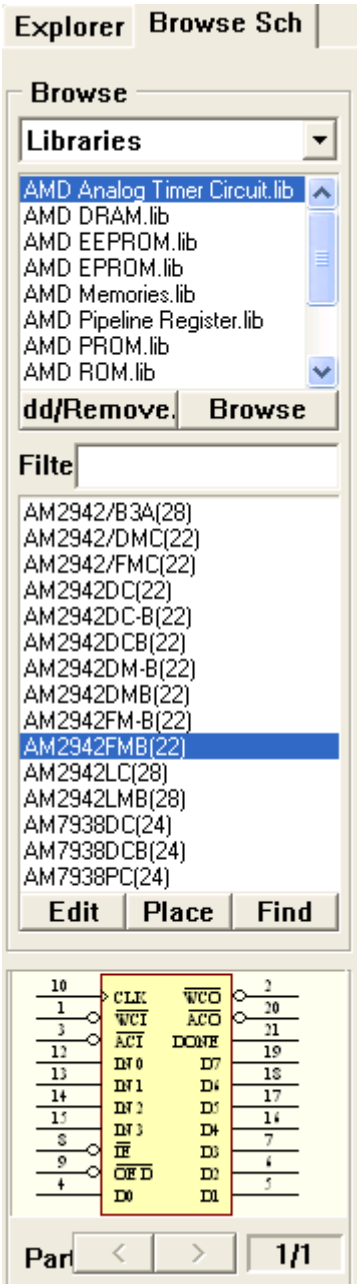
Design Explorer 99 SE\Library\Sch folder in your Protel installation directory.

New libraries are constantly being developed by the Protel Library Development Center. Visit the PLDC on the web at www.protel.com for the latest downloadable libraries.

Each schematic component then consists of one or more parts, which represent the functional devices contained within the component. For example, a 74LS00 contains four parts (AND gates), a capacitor has one part, and a relay can be made up of a coil part and a contact part.

Components are created and modified in the schematic library editor, an independent document editor that includes tools for managing and editing libraries. You can open a schematic sheet the schematic library editor simultaneously, with special features to link between sheet and library operations. For example, you can move directly from a part symbol on the sheet, to editing its component information inside the source library.

Making schematic libraries available for use



To access the components in the schematic libraries, the libraries must first be added to the list of available libraries in the schematic sheet editor.

To view a list of currently available libraries, set the Browse scope to Libraries in the schematic panel. A list of currently loaded libraries will be shown. Click on a library name in the list to show a list of all components it contains in the lower list box.

To add libraries to the available libraries list, click the Add/Remove button on the panel, or select Design→Add/Remove Library from the menus. This opens the Change Library List dialog, where libraries can be added and removed from the Current File List. The only limit on the number of libraries that can be added is the memory available in your computer. Once libraries have been added, parts from those libraries can be placed on the sheet.

The default schematic libraries supplied with Protel 99 SE are stored within a series of design databases (.DDB files) located in the Design Explorer 99 SE\Library\Sch folder in your Protel installation directory.

Each design database may include a number of individual schematic libraries. Selecting a design database adds all the libraries it contains to the available libraries list.

Finding components within schematic libraries

Protel 99 SE includes the ability to search all schematic libraries in a predefined path for a component.To find a component in a library, when a schematic sheet is active press the Find button on the schematic editor panel, or select Tools→Find Component to pop up the Find Schematic Component dialog.

Following are some tips on searching for components:

1. If possible, search by Library Reference as it is much faster. Also the way you describe a component may not be the way it has been described in the library.
2. Include the * wildcard before and after the library reference, as different manufacturers use different prefix and suffixes.
3. If your search produces no results check that the Path is correctly specified. Also, try searching for a component that you know is in a library to check that everything is set correctly.
4. Use the Add to Library List button once you locate the correct component to add the library to the available libraries list.

Browing component libraries

You can browse for schematic components in the schematic panel, using the MiniViewer that appears at the bottom of the panel when the Browse mode is set to Libraries. You can also browse schematic component libraries in the Browse Components dialog (Design→Browse Library).

Placing parts from schematic libraries

To view a list of currently available components, from the schematic document set the Browse scope to Libraries in the schematic panel . A list of currently loaded libraries will be shown in the top list box. Click on a library name in the list to show a list of all components it contains in the lower list box.

Select a component in the lower list box of the schematic panel and press the Place button.

Part 9 Editing schematic component libraries

Schematic component descriptions are stored in schematic libraries, which can be stored within or linked to a design database, or stored as external files named with a .LIB extension. The default schematic libraries supplied with Protel 99 SE are stored within a series of design

databases located in the Design Explorer 99 SE\Library\Sch folder in your Protel installation directory.

Schematic libraries are managed using the schematic library editor, which is used to create and modify the components symbols and descriptions contained within schematic libraries.

To be able to edit a schematic library in Protel 99 SE, it must be stored in or linked to a Protel design database.

To edit a schematic library, use the Design Explorer to open the design database containing the library or library link. Design databases that contain schematic libraries can be manipulated as you would any other design database.

Simply use the Design Explorer to open a stored or linked schematic library as a document within the design database. Schematic library documents are automatically opened with the schematic library editor.

Creating a new schematic library

To create a new schematic library, first open or create a design database in which to store the library.

To create a new schematic library, from within a design database select File→New, and double click on the SchLib icon in the New Document dialog. A new empty schematic library document will be created in the current folder of the design database. To open the library,

double-click on its icon in the design window, or click on its icon in the navigation tree.

As a library is a set of components, it can not exist without at least one component. When you create a new library, an empty component sheet (called Component_1) is also created within the library. To rename Component_1 with a name of your choice, open the library, select Component_1 from the list in the schematic library editor panel, and select Tools ?Rename Component from the menus.

Editing components in schematic libraries

Within each schematic library are a set of components. Each component within the library consists of one or more parts. The component represents the physical device, and the parts represent the functional devices it contains. For example, a discrete resistor component would have just one part, whereas a resistor network might have eight parts, each representing a single resistor within the physical resistor network package.

The partitioning of components into parts is entirely up to you as the designer. You may wish to draw the coil of a relay as one part and the contacts as another, or it might be more appropriate to draw the whole relay as one part. A four pin connector could be drawn as one part, or it could be drawn as four parts. Each part of a component is drawn on a

separate sheet within in the schematic library editor.

As well being able to have more than one part, each part can have up to three graphical representations, or modes; Normal, De-

Morgan and IEEE. Each mode is drawn on a separate sheet. The preferred mode is selected when the part is placed on the schematic sheet, with the default being normal. Only the Normal mode must be created, the other two are optional.

Part 10 Repositioning design objects on a schematic

In Protel schematic documents there are two main ways of repositioning design objects: objects can be moved or dragged.

1. Moving an object changes its position on the sheet without maintaining connectivity. Any connect wires are not moved with the object and any connections will be broken.
2. Dragging an object change its position on the sheet whilst maintaining connectivity. Any connected wires are moved with the object being dragged so that the connectivity of the schematic is maintained.

Moving and dragging can be performed on single objects, or on selected groups of objects.

To move a single object or selection, from the schematic select Edit→Move→Move or Edit→Move→Move Selection from the menus to enter move mode. The cursor will change to a crosshair. Left-click on an object (or any object in a selection) to "pick up" the object. Move the cursor to reposition the object(s) and left-click or press ENTER to place the object. Right-click or press ESC to exit move mode.

To drag a single object or selection, repeat the above procedure, but select Edit→Move →Drag or Edit →Move →Drag Selection from the menus.

To align selected objects on both axes, from the schematic select Edit ?Align ?Align to open the Align Objects dialog [shortcut A A]. Select the desired vertical and horizontal alignment from the option buttons and click OK to have all selected objects moved to the chosen horizontal alignments. Enable the Move Primitives to Grid option to constrain alignment to the nearest grid point.

The following single-axis alignments are available from the Edit →Align submenu or via shortcut keys:

Align Left CTRL+L

Align Right CTRL+R

Center Horizontal CTRL+H

Distribute Horizontally CTRL+SHIFT+H

Align Top CTRL+T

Align Bottom CTRL+B

Center Vertical CTRL+V

Distribute Vertically CTRL+SHIFT+V

Part 11 Wiring up a schematic

Wiring up a schematic is the process of placing wires, buses ports and net labels on your schematic to define the connectivity of the circuit. The following topics discuss wiring up a single schematic sheet. See the Creating projects with multiple schematic sheets topic in the Links section below for information on connectivity in multi-sheet designs.

Overview of connectivity in schematics sheets

Connectivity is the ability to recognize the physical links between objects inside a schematic sheet and to associate logical connections that exist between various sheets in a multi-sheet design. Connectivity is also used to anchor certain objects together. For example, you can drag connected electrical items (parts, buses, wires, ports, etc.) without breaking existing connections. More importantly, connectivity allows the schematic to generate netlists and perform electrical rule checks.

Connectivity is derived from the placement of certain electrical objects in the sheet and from the placement of net identifiers. However,

not all electrical objects use placement to define connective behavior. Some objects use their geometry to establish physical connectivity. Other objects include logical connectivity in their behavior.

Electrical objects are connected when their electrical "hot spots" are touching. When the electrical grid is enabled (Design→Options) the cursor will jump to the nearest hot spot and change into a "dot" shape, indicating a valid electrical connection can be made.

Special cases of connectivity are:

Wire to Wire: Wires whose ends touch at any angle, butt end-to-end or have co-linear (overlapping) terminations are deemed to be connected. Co-linear wires that terminate elsewhere on the sheet are not deemed to be connected. Wires that cross or terminate perpendicularly are not deemed to be connected unless a junction is placed at their intersection.

Net Label to Wire: Net labels associate a wire with single net. To achieve this association, the net label must be placed on the same grid point as the wire, either vertically or horizontally. Labels can only be placed on horizontal or vertical lines or at line vertices.

Wire to Bus: Buses are graphical representations of grouped signals, and do not have any special connective properties for netlisting. Although buses display hot spots when wiring and maintain connections during drags, they do not simulate electrical connections. Wires are graphically connected to buses using bus entry symbols. Net labels must be used to

indicate logical connectivity on either side of the bus connection.

Net Label to Bus: Buses are graphical entities and do not provide physical connectivity for netlisting. Logical connectivity for buses can be assigned by placing a net label on the bus. Generally, this net label will include all bus signals, e.g. HA[0..19] represents nets named HA0, HA1, HA2, etc. to HA19. Buses and bus entries do not highlight when the *Edit »Select » Net* process launcher is used.

Wire to Pin: Pins that touch the ends of wires at any angle are deemed to be connected. Pins that intersect perpendicular wires must be connected by placing a junction at that location. Junctions will be automatically inserted where wires cross pins perpendicularly when this option is active (Tools »Preferences menu item).

Pin to Object: Pins connect directly to other pins, wires, net labels, sheet entries or ports. Hidden pins can be assigned directly to nets in the Schematic Library Editor. Unhidden pins can also connect directly to other sheets, when that sheet is named in the part's Sheet Path field.

Wire to Port: A Wire touching the end of a port is deemed to be connected.

Pin to Pin: Pins are deemed to be connected if they are in contact at any angle.

Bus to Object: Buses are graphical representations of grouped nets only and have no special physical properties for netlisting. Logical

connectivity (use of net identifier, e.g. net label and port) is used in these cases to indicate connections on either side of a bus. Note however, if a bus is connecting to a port the bus line must end on the end of the port.

Wire to Sheet Entry: A Wire touching the end of a sheet entry is deemed to be connected.

No ERC: No ERC objects are deemed to be connected to pins or wires if they are in contact.

Two other special classes of electrical objects are provided. Directives: used to indicate; simulation points, unconnected pins (No ERC) and PCB layout properties on individual nets. Net identifiers: used to indicate electrical connections that are not physically wired together, eg. connections that continue from one schematic sheet to another in a multi-sheet design.

The process of placing electrical objects in the sheet is often referred to as wiring. This is because the connectivity features allow you to work with electrical objects as though you were physically hooking-up the circuit.

Net identifier objects support connections that are not physically joined by wires. These objects include: net labels that identify common nets on a sheet (or globally, across multiple sheets if you specify); ports that identify net connections between two sheets; sheet entries that identify net connections into a sub-sheet (referenced by a sheet symbol);

and power ports which are special symbols placed to represent a global power (or another user-specified) net.

Hidden pins on parts are a special fifth type of net identifier that function similarly to power ports. Hidden pins connect to all other hidden pins with the same name and connect to a net of the same name, if present. If "unhidden" these pins are not deemed to be connected and must be manually wired to be included in a netlist.

Schematic guided wiring and auto-junctioning

Protel's schematic editor includes two features to help you place wires to electrically connect schematic objects

Guides Wiring: Schematics have a definable electrical grid that makes it easy to make electrical connections between objects. As you are placing a wire, when the wire falls within the electrical grid range of another electrical object, the cursor will snap to the fixed object and a Hot Spot (highlight circle) will appear. The Hot Spot guides you to where a valid connection can be made and automatically snaps the cursor to electrical connection points. It is recommended that you set the electrical grid to be set slightly smaller than the current snap grid, or it becomes difficult to position electrical objects one snap grid apart.

Auto-junctioning: The schematic auto-junctioning feature automatically places an electrical junction when one wire is terminated

(ends) on the body of another wire (in a "T" junction), or when a wire connects orthogonally to a pin or power port. This allows you to easily create electrical connections at junction points without the need to manually define the connection. Wires that cross away from their end points do not have a junction is inserted.

The auto-junction feature is enabled of disabled in the Schematic tab of the schematic Preferences dialog (from a schematic select Tools→Preferences).

Setting the schematic auto wire mode options

When placing wires or buses in a schematic, a special auto wiring mode is available to automatically route wires and buses between points on the schematic.

When the auto wiring mode is active during wire or bus placement, press the TAB key to open the Point To Point Router Options dialog, which allows you to set the auto wiring options. The following options are available:

1. Clearance: Defines the minimum clearance between the wire and other objects on the sheet.
2. Time Out After (s): Sets the maximum time in seconds that the autowirer will try to calculate a path. If it cannot find a routing path within this time, it will stop and no wire will be placed.

3. Avoid cutting wires: The setting of the slider determines how hard the autowirer will try to avoid cutting crossing existing wires.

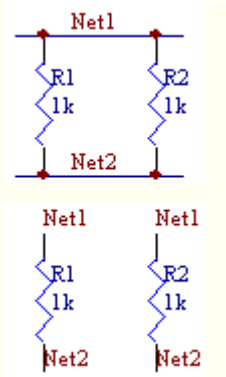
Connecting schematic objects using net identifiers

In connectivity terms, a net defines electrically connected points in a circuit. By placing a wire between two nodes in a schematic, you effectively assign the two points to the same net. In a schematic, Protel internally assigns a unique name to each net in the circuit, but you can manually define net names to create connectivity between nodes on the schematic.

To manually assign a net name (or net identifier) to a point in your schematic, place a Net Label on that point. The net name is the name given to the Net Label.

If you assign the same net name two or more points on a schematic, these points are effectively connected electrically. You do not need to manually connect them using a wire.

The diagram (left) shows two electrically equivalent circuits. The top shows two resistors connected in parallel using wires to make the connections. The bottom shows two resistors connected in parallel using net labels to define the connections



A typical use of connections using net identifiers is

connecting to power nets. When you place a power port on a schematic it defines a net which has a net name equivalent to the power object's name (VCC, GND, etc.). You can then place net labels on any schematic circuit nodes which have the same net name as the power port to automatically connect these nodes. You do not need to physically wire the nodes to the power port.

Part 12 Workspace editing techniques

The schematic editor includes a number of features to make the design process more productive. These include:

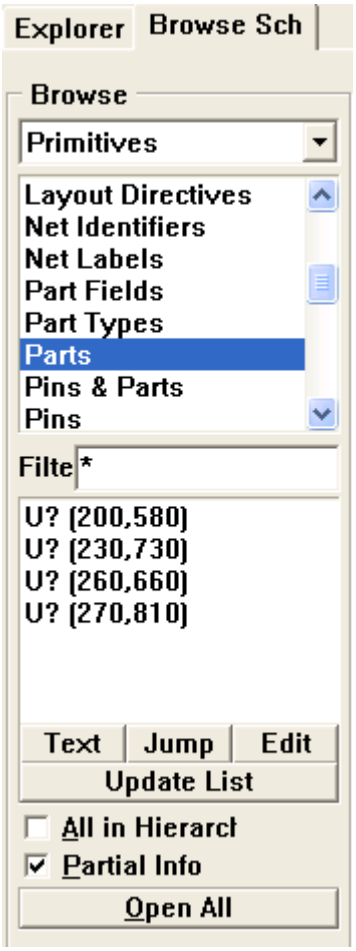
1. Jumping around the workspace

To move quickly around the current schematic sheet select Edit→Jump from the schematic menus to open the Jump submenu.

2. Browsing with the panel

When a schematic document is active, the schematic editor panel can be used to browse through and locate the various objects on the current sheet, or the entire schematic project. Select Primitives in the pull-down list, then select the type of objects you wish to browse. A list of all objects of the selected type will appear in the list window.

You can filter this list by including a text mask (using the * and ? wildcard characters) in the Filter field.



Select an object in the list and then:

- Click Jump to jump to the selected object, centering it in the design window.
- Click Text to jump to the selected object and edit its text field, if applicable.
- Click Edit to jump to the selected object and edit its properties.
- Click Update List to refresh the browse list.

Enable the Whole Project option to include objects from all connected schematic sheets. Disable this option to limit the browse list to the active sheet.

Enable the Partial Info option to show only the names of the objects in the object list. Disable this option to show full details of the objects in the list window.

3. Morphing, or inheriting properties

Protel 99 SE's schematic editor has a powerful feature for copying the properties of one object into a second object of the same type. You can use this feature whenever you have an object floating on the cursor before placing it.

4. Finding and replacing text

Protel 99 SE allows you to find and replace text anywhere on a single schematic sheet, or across a multi-sheet project.

To find text, select Edit→Find Text from the menus.

To find and replace text, select the Edit→Replace Text from the menus.

5. Pasting arrays of objects

When a schematic object is on the schematic clipboard , it can be pasted into the schematic as an vertical or horizontal object array.

To do this select Edit→Paste Array from the schematic menu to open the Setup Paste Array dialog. In this dialog, the following options can be set:

Item count - the number of copies of the clipboard object(s) to paste.

Text increment - an integer defining the designator number increment for each Part object that is pasted.

Horizontal spacing - the horizontal spacing distance to the right between each pasted array object. If set to 0, pasted objects are in a vertical line.

Vertical spacing - the vertical spacing distance above each pasted array object. If set to 0, pasted objects are in a horizontal line.

Once you have set the options in the Setup Paste Array dialog, click OK to close it. Position the cursor where you want to insert the array and left-click or press ENTER to past the objects.

Part 13 Creating projects with multiple schematic sheets

Protel 99 SE supports single sheet, multiple sheet and fully hierarchical schematic designs, including complex hierarchy, where multiple instances of a single sheet can be used in a project. There is no limit on the number of sheets that you can have in a design.

Multiple sheet projects support large or complex designs that cannot be served by a single sheet. Even when the design is not particularly complex, there can be advantages in organizing the project across multiple sheets. For example, the design may include various modular elements. Maintaining these modules as individual files allows several engineers to work on different parts of the design at the same time.

The relationship between sheets in a multi-sheet design is formed by a special symbol called a sheet symbol, which provides a graphical representation of subsheets in the design. Sheet symbols contain ports that represent links on the source schematic. Placing a sheet symbol on a schematic links that schematic to the sheet represented by the sheet symbol.

Before creating a multi-sheet schematic design, it is important that you understand how net identifiers are treated across the design, and the

different hierarchy models that can be used to electrically link net identifiers in multiple sheets. This will affect the way you name nets, power ports, etc. in the different sheets of a multi-sheet design.

Linking schematic sheets using sheet symbols

Protel's schematic editor includes features to "automate" the process of creating and linking multi-sheet projects. When you start a multi-sheet project you adopt either a "top down" or "bottom up" approach to the design, or a mixture of both.

Top-down design involves defining the functional blocks of your circuit as sheet symbols on a master schematic, and then creating the schematics. If you adopt this approach, you can select Tools ?Create Sheet From Symbol from the schematic menus to automatically create the schematic subsheets based on the sheet symbols you have created. You will be prompted to select a sheet symbol. After clicking on a sheet symbol a new schematic sheet will open with the correct file name. The new sub-sheet will include ports to match each of the sheet entries on the sheet symbol you selected.

Bottom-Up Design involves creating the various schematics as independent circuits, then creating sheet symbols based on these schematics, then linking these sheet symbols on a master sheet to create

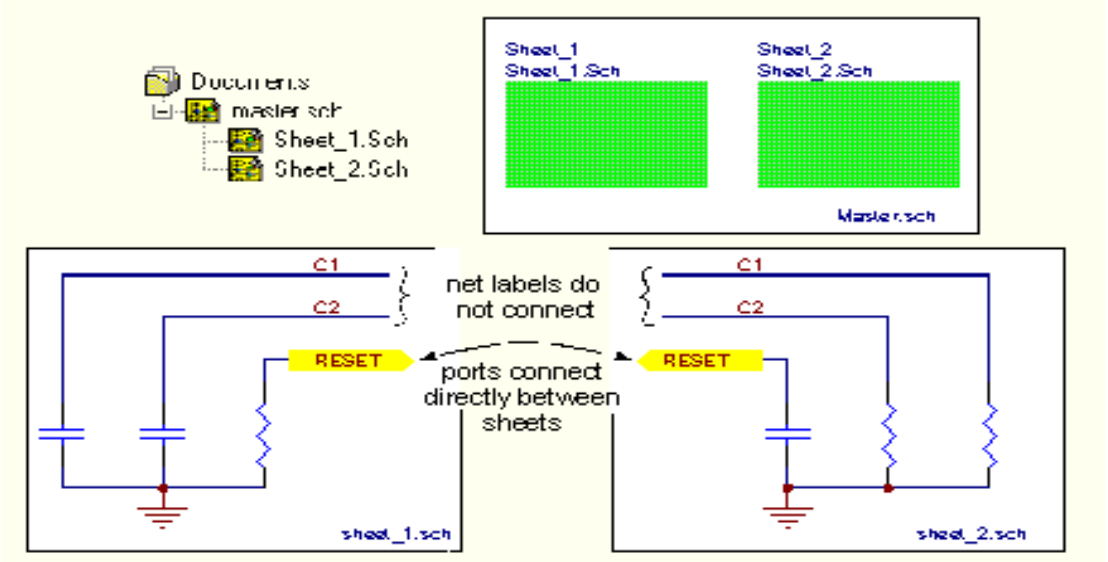
the final design. If you adopt this approach, select *Tools »Create Symbol From Sheet* from the schematic menus (the intended parent sheet must be the active sheet). The Choose Document to Place dialog will open with a list of all schematic sheets available in the same folder as the active sheet. Select the sheet you would like to base your sheet symbol on. You will then be asked if you want to Reverse Input/Output Directions. After you answer this (see below), you will be presented with a sheet symbol floating on the cursor. This sheet symbol will have sheet entries to match each of the ports on the selected subsheet.

Each of the ports on the sub-sheet has an I/O type. Say one of the ports has an I/O type of output. If you respond "yes" to the Reverse Input/Output Directions question then the sheet entry that matches this port will have an I/O type of input (the I/O direction has been reversed) and will be positioned on the left of the sheet symbol. If you respond "no" to the Reverse Input/Output Directions question then the sheet entry that matches this port will have an I/O type of output and will be positioned on the right of the sheet symbol.

This is called a "flat" design as all the sub-sheets are on the same level in the project hierarchy. The top sheet includes the sheet symbols for all the sub-sheets, but not any wiring or circuitry. In this model all the inter-sheet connection are made globally through ports, where ports of the same name are connected throughout the project. Note that the net names

in the two sub-sheets are local, meaning that the net name connects only within each sheet, not to other sheets in the project.

Management of large designs with this model can be awkward because it is difficult to trace a net from one sheet to another.



To use this model for multi-sheet schematic designs, set the Net Identifier Scope to Ports Only Global when performing an ERC, running a simulation, creating a netlist, compiling a schematic-based PLD, or synchronizing between schematic and PCB documents.

This model is referred to as complex hierarchy. In this model the same sheet symbol can be placed more than once in a project, either by being placed more than once on a single sheet, or by being placed on multiple sheets. This model fits projects which are highly modular. For example, a stereo amplifier, where left and right channels are identical circuits.

Complex hierarchy is used during the schematic capture phase. When

you are performing any electrical analysis on this type of multi-sheet design you must first "flatten" the design, converting it from complex to simple. From the schematic, select Tools→Complex to Simple to flatten the design. Each child sheet that is used more than once will be copied and renamed. You must also re-annotate the design to assign a unique designator to each part.

To use this model for multi-sheet schematic designs, set the Net Identifier Scope to Sheet Symbols / Port Connections, when performing an ERC, running a simulation, creating a netlist, compiling a schematic-based PLD, or synchronizing between schematic and PCB documents, after first converting the design from complex to simple.

Part 14 Schematic design verification - the ERC

Design verification is the process of ensuring that the schematic capture process has produced an accurate "snap shot" of your design, from which a valid netlist can be created. In Protel's schematic editor this is done using the Electrical Rule Checker (ERC). This process examines the schematic for both electrical inconsistencies, such as an output pin connected to an output pin, and drafting inconsistencies, such as unconnected net labels or duplicate designators.

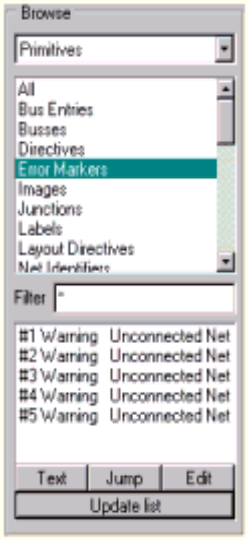
From a schematic document, select Tools ?ERC from the menus to

open the Setup Electrical Rule Check dialog. This is used to set-up and execute the Electrical Rule Check.

Running the ERC produces two results. First, a text report is generated, listing the electrical and logical violations either for the active sheet, or the entire project. Secondly, error markers are placed on the sheets at the site of each ERC violation as an aid in tracking and correcting reported problems.

There may be points in the design which you know will be flagged as ERC errors or warnings, which you do not want to be flagged. To suppress these, place a No ERC schematic directive objects at each point (Place→Directive →No ERC).

Browsing ERC errors on a schematic sheet



After you have run an ERC on a schematic, any warnings or errors are shown as Error Marker objects on the schematic. You can easily identify all ERC errors in a schematic by using the schematic panel to browse through the Error Markers.

In the panel, set the Browse scope to Primitives and select Error Markers from the top list box. A list of all error markers will appear in the bottom list box. Select an error in the list and press the Jump button to have the error marker presented in

the center of the active window.

Note that a description of the error condition appears on the Status Bar, alleviating the need to switch back and forth to the error report. Pressing the Text button in the Component Browser will pop up a dialog which can also be used to examine the description of the error condition.

Typical causes of schematic ERC errors

Errors found when performing an Electrical Rules Check (Tools→ERC) on a schematic will typically be due to the one or more of the following conditions:

- Drafting errors - wires overlapping pins, lines being used instead of wires, the design being wired with the snap grid off so the wire ends don't touch the pin ends or wires / busses finishing under a port instead of touching the end of the port.
- Syntax errors - net identifiers with spelling mistakes or busses incorrectly labeled.
- Component errors - component pins placed the wrong way around on the component or pins with an inappropriate Electrical Type.
- Design errors - a design condition that the ERC detects as an error, such as two output pins connected.

Printing and plotting a schematic

Protel 99 SE includes support for a wide variety of hard copy options for schematic sheets. Virtually any device that is supported by Windows can be used to print or plot your schematic drawings.

Schematic printing and pen-plotting are handled similarly to other Windows applications. Windows manages the printing (or plotting) process and provides a range of raster and PostScript printer drivers and vector plotter drivers. These range from 9 pin dot matrix printers and multi-pen plotters, to high-resolution raster imagesetters.

To setup to print or plot from the active schematic or schematic library, select the File→Setup Printer menu item. This will open the Schematic Printer Setup dialog, allowing you to choose a printer and set up the output options.

To start the print process, click the Print button in the Schematic Printer Setup dialog, or from a schematic select File→Print from the menus.

Unit 6 Working in PCB documents

A printed circuit board (PCB), sometimes referred to as printed wiring board (PWB), is the foundation of circuit construction. Components are soldered onto the PCB, and the PCB provides the electrical connection pathways between components to form the physical circuit. Connections are made using copper tracks etched onto the various layers of the PCB. A PCB document is displayed as a set of superimposed layers, with each layer corresponding to an individual "phototool" used to fabricate the board.

In general, a PCB is derived from a schematic representation of the circuit. When a schematic is loaded into a PCB document, schematic part symbols are translated to corresponding board component footprints, and the connectivity of the schematic is preserved and displayed as connection lines in the PCB document.

Part 1 PCB design objects

A variety of objects are available for use in designing a PCB. Keep in mind that most objects placed on a PCB document will define copper areas or voids in the physical PCB. This applies to both electrical objects,

such as tracks and pads, and non-electrical objects, such as text and dimensioning. It is therefore important to keep in mind the width of the lines used to define each object, and the layer that the object is placed on.

The topics listed below give a full description of each available design object in this toolbar.

1.Arc

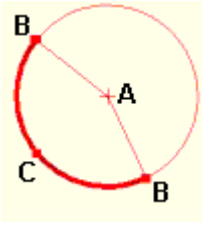
Toolbar: 

Valid Layers: All

Can be connected to a net?: Yes

An arc is essentially a curved track segment and can be used to produce curved paths during routing, or curved component or board outlines. During board routing, arcs are placed on the board when in the "Arc Corner" placement mode.

There are two methods for placing arcs on a PCB: Center or Edge placement. In each case you define a number of points on the arc in



sequence by positioning the cursor and left-clicking or pressing the ENTER key. When you complete the sequence the arc will be rendered and you can begin placing another arc. Right-click or press ESC to exit the arc placement mode.

When an arc is in focus, the following editing handles are available : Point A marks the center of the arc. Click to "grab" the arc by its center and move it. You can also move the arc by clicking anywhere on the arc itself.

Click B to change the start and end points of the arc.

Click C to change the radius of the arc.

2. Component Footprint

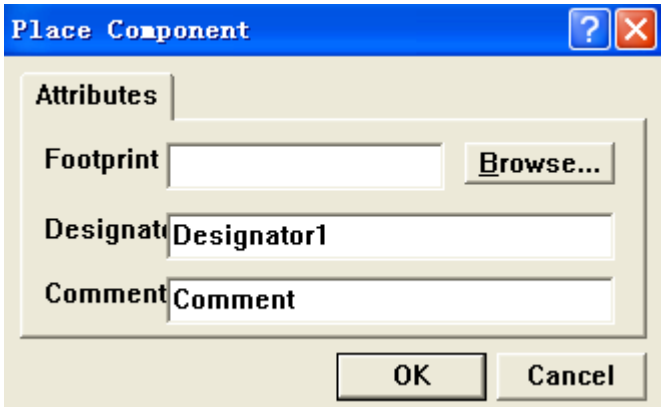
Toolbar: 

Valid layers: Top or Bottom signal layers

Can be connected to a net?: No (Component pads, however, can be assigned to net)

A component footprint is the representation of a physical device on a PCB. A footprint may contain pads for connecting to the pins of a device, a physical outline of the package, device mounting features, etc.

When you enter component placement mode the Place Component dialog will open.



In this dialog, type the name or browse for a component footprint from a loaded PCB library. Set the appropriate designator and any comment text, then click OK to close the dialog. You will return to the PCB document and an outline of the component will be "floating" on the cursor. Position the component and left-click or press ENTER to place it. The Place Component dialog will re-open, allowing you place another component. Press Cancel to exit component placement mode.

3. Fill

Toolbar: 

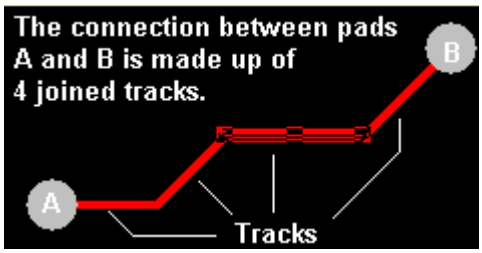
A fill object places a solid rectangular block on the current PCB layer.

4.Track - Interactive Routing

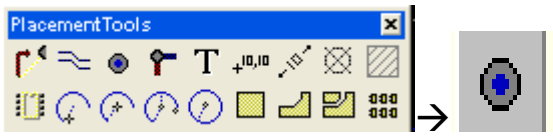
Toolbar: 

Interactive routing is the process of placing track segments. A track

is a straight solid-filled line with a defined width. Tracks are generally placed on a signal layer to form the electrical interconnection between component pads on a PCB. However, tracks are also used as general-purpose line drawing elements to create board outlines, components outlines, polygon planes, keep-out boundaries, etc.



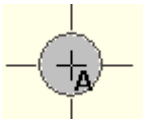
5.Pad

Toolbar: 

Pad objects are normally used to create connection pads for component pins.

In pad placement mode simply position the cursor and left-click or press ENTER to place a pad. Continue placing further pads, or right-click or press ESC to exit pad placement mode.

When a pad is in focus, the following editing handles are available :



Point A marks the center of the pad. Click here to "grab" the pad by its center and move it to a new location. You can also move a focused pad by clicking anywhere within the pad border. This will "grab" the pad at the point at which you click.

6.String

Toolbar: 

Can be connected to a net?: No

The string object places text on the selected PCB layer. As well as user-defined text, special strings can be used to place board or system information on the PCB, such as the layer name or a board legend, by setting the string text to be one of the special string names (see the Links section below for more information).

Part 2 PCB design layers

A PCB is fabricated as a series of layers, including copper electrical layers, insulation layers, protective masking layers, and text and graphic overlay layers.

There are 2 types of electrical layers -signal layers, which contain the signal interconnect paths, and power planes, which are layers of unbroken copper used to distribute current to power the components.

Protel's PCB editor provides for the design of boards with up to 32 signal layers plus 16 internal plane layers. These signal and plane layers are made available in the workspace by defining the layer stack-up, which

is defined in the Layer Stack Manager dialog Design (Layer Stack Manager). As well, additional special layers, such as solder and paste masks, mechanical drawing layers, drill layers, etc, are available.

The 16 mechanical layers have a special property in that they can be added to any other layer during print or plot output generation. As well, objects placed on a special Multi layer will automatically be added to each signal layer.

Protel’s PCB editor is a "layered" environment. You create your board design by placing objects on these layers. These layers are either "physical" layers, from which the fabrication information is created, or system layers, such as the Connect layer which displays the unrouted connections. Physical layers include the signal layers, internal plane layers, silkscreen, solder mask and paste mask layers.

Before you can place objects on a physical layer in your PCB document, that layer must be turned on. Once a physical layer is turned on, a Layer Tab for that layer will be displayed at the bottom of the PCB document pane in the design window.

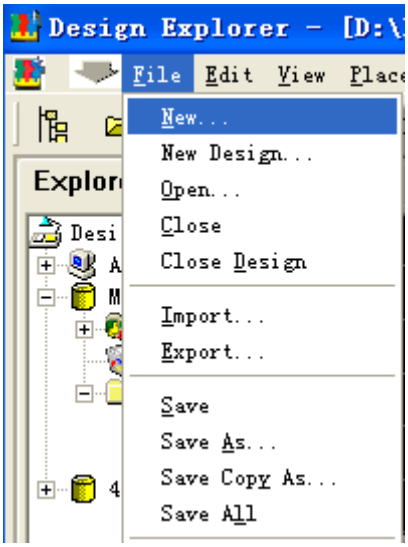
To display or hide particular layers from a PCB document select Design >Options from the menus and activate the Layers tab in the Document Options dialog [shortcut L]. For each of the layers there is a check box next to the layer name, a tick in the check box indicates that this layer is visible. Layer colors are defined in the Colors Tab of the

Preferences dialog, select Tools ?Preferences to display this dialog.

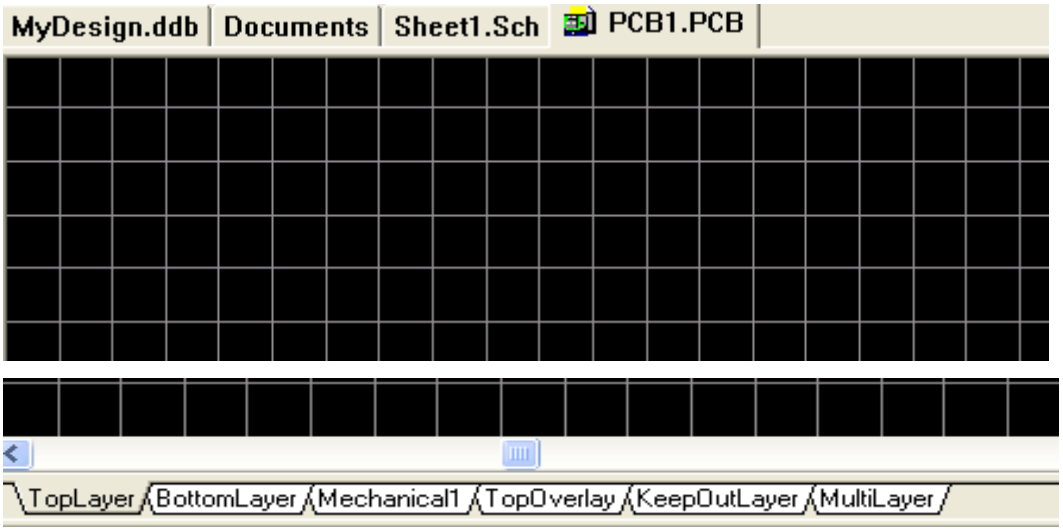
Note: Signal and plane layers will only be listed in the Document Options dialog if they have been enabled in the Layer Stack Manager dialog. Mechanical layers will only be listed if they have been enabled in the Setup Mechanical Layers dialog.

Part 3 Defining a new PCB

To begin the PCB design phase of a project, create a new PCB document in your design database.



Then select OK, you will see the following board, and creat a new PCB called PCB1.PCB. In the bottom of the board, you can see the six layers .



Before bringing design information from the schematic, you should first create the mechanical and electrical board outline for your board, and configure the layer stack.

The mechanical outline defines the physical shape and size of the board, and also includes items such as dimension detail, photo tool targets

and other company and fabrication specific information. This information is usually placed on the four Mechanical layers.

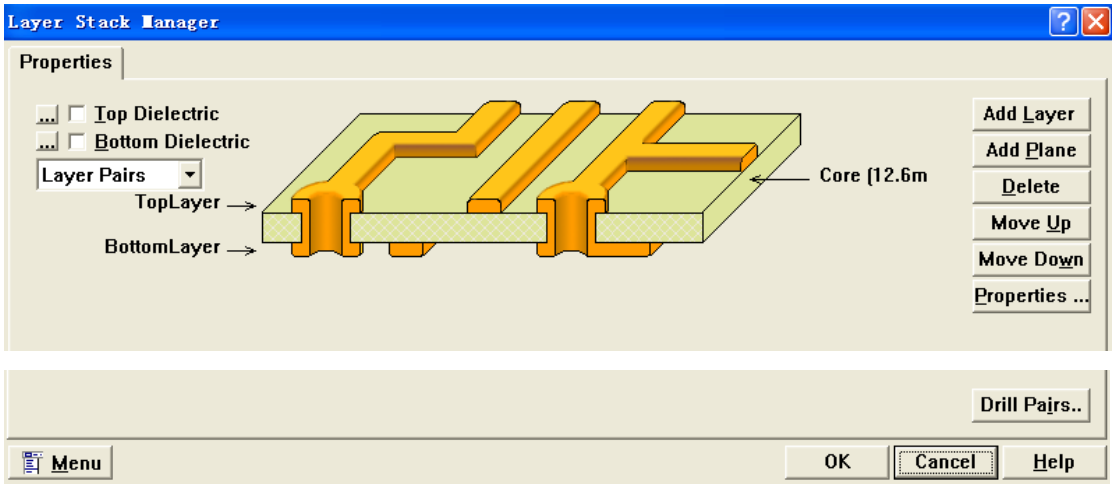
The electrical board outline defines the routing and component placement limits of the board. This is done by defining an outline of the board on the Keep Out layer. The Keep Out layer is a special layer that allows you to define "legitimate" placement and routing areas in the PCB workspace. Generally you would define an area which is the same as the physical board outline. All signal-layer objects and routing would then be confined within this area. You could also define areas on the Keep Out layer within the board outline to act as "no go" areas for placement and routing.

The layer stack defines what signal and plane layers are available. Part of the layer stack definition process is to define the drill-pairs.

Protel 99 SE includes a powerful Board Wizard that guides you through the complete process off creating a new PCB document and board definition. The Wizard include a number of pre-defined board templates, and allows you to create your own templates.

Defining the PCB layer stack

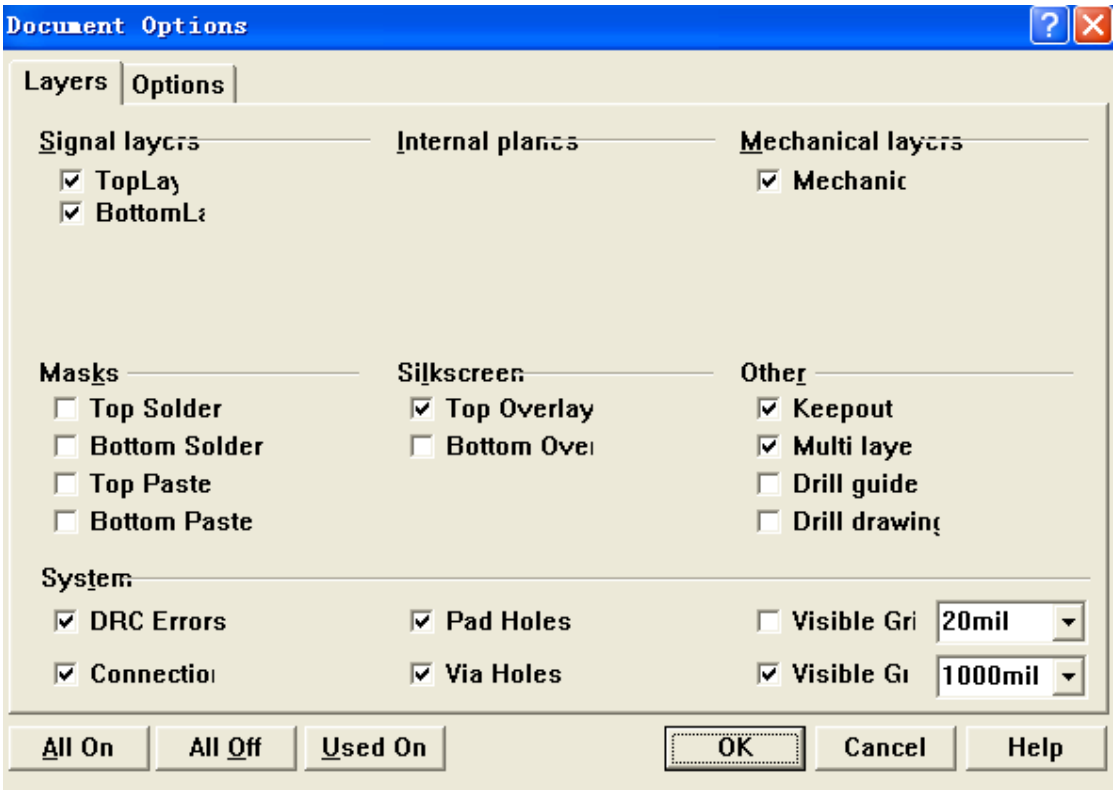
The layer stack is defined in the Layer Stack Manager dialog (Design >Layer Stack Manager)



The image in the center of the dialog shows the current layer stack, the default is for a double-sided board. New layers can be added to the design by clicking on the Add Layer and Add Plane buttons. Each new layer is added below the layer that is currently selected. Double-click on a layer name to edit the properties of that layer.

The Menu button at the bottom of the dialog includes a number of pre-packed example layer stacks. Note that these example layer stacks are not fixed, you can start with one of these and easily modify it. Once the required layers have been added, use the Move Up and Move Down buttons to configure the layer stack. New layers can be added at any point in the design process.

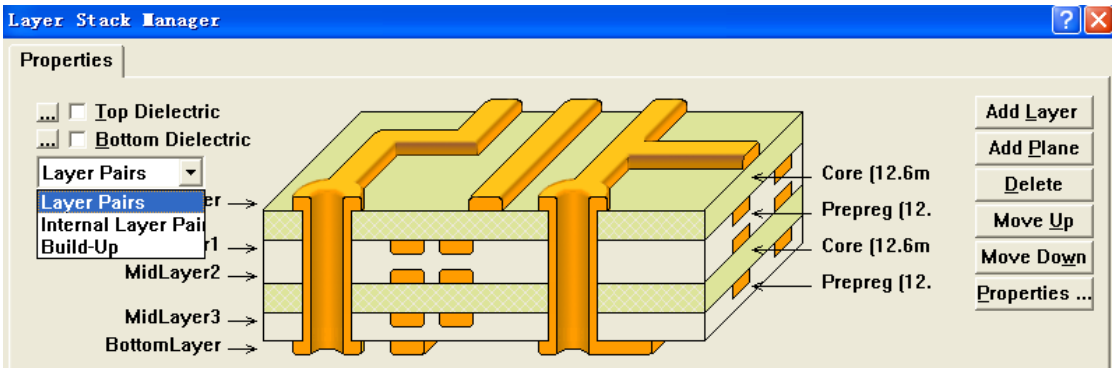
There are a total of 32 signal layers available (top layer, bottom layer, and 30 mid-layers) and 16 plane layers. Layer visibility is controlled in the Document Options dialog (Design >Options).



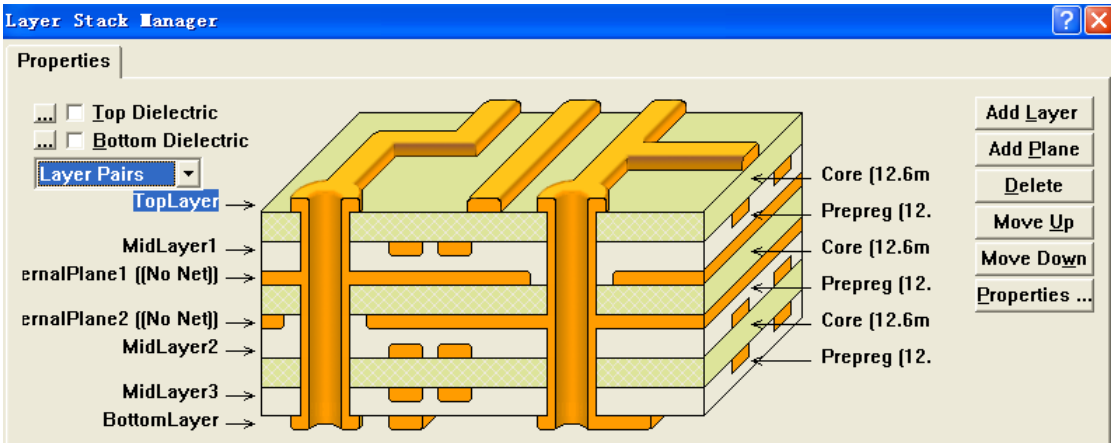
Selecting the Layer Stack-up Style

As well as the electrical layers, the stack-up includes the non-electrical insulation layers. There are typically 2 kinds of insulation used in the fabrication of a PCB, usually referred to as core and prepreg.

The stack-up style refers to the order of the insulation layers through the layer stack. Three default stack-up styles are supported **-layer-pairs, internal layer-pairs, and build up**. Changing the layer stack-up style changes the way that the core and prepreg layers are distributed through the layer stack.

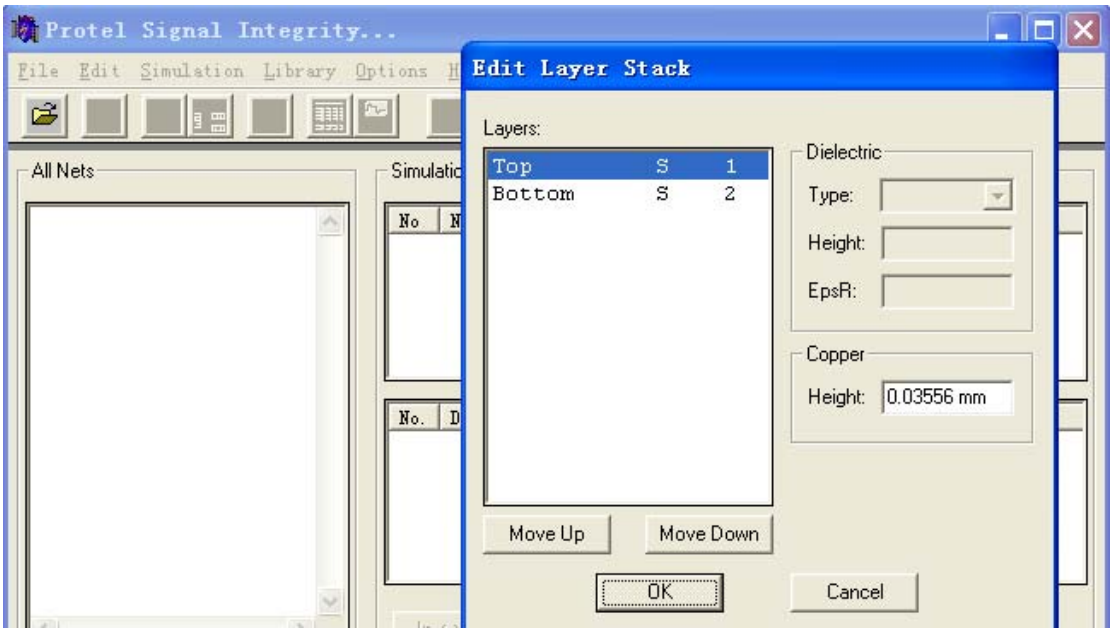


Select the preferred stack-up style at the top left of the Layer Stack Manager dialog. Defining the stack-up style is required if you plan to use blind and buried vias, and for signal integrity analysis. If you are planning to use blind and buried vias you must consult with your PCB manufacturer to ensure that that they can fabricate the design, and that the correct stack-up style is selected.



Defining the layer properties

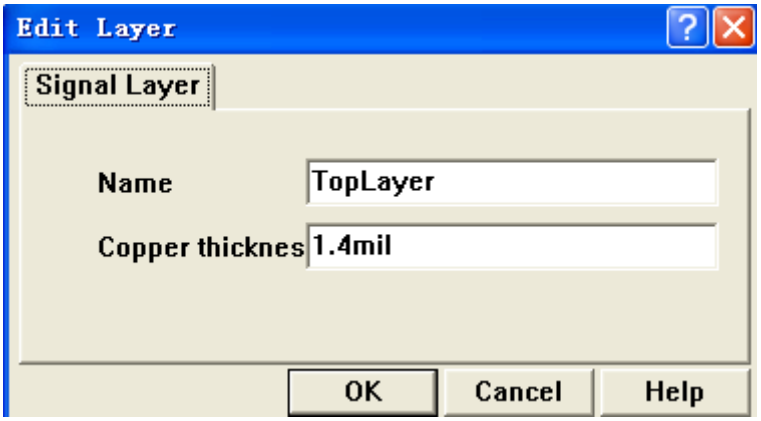
There are 3 kind of layers added to the layer stack in the Layer Stack Manager, signal layers, plane layers and insulation (substrate) layers. The information in these dialogs must be correctly specified if you intend to perform a signal integrity analysis (Tools>Signal Integrity).



Signal layers

Name -- User-defined layer name

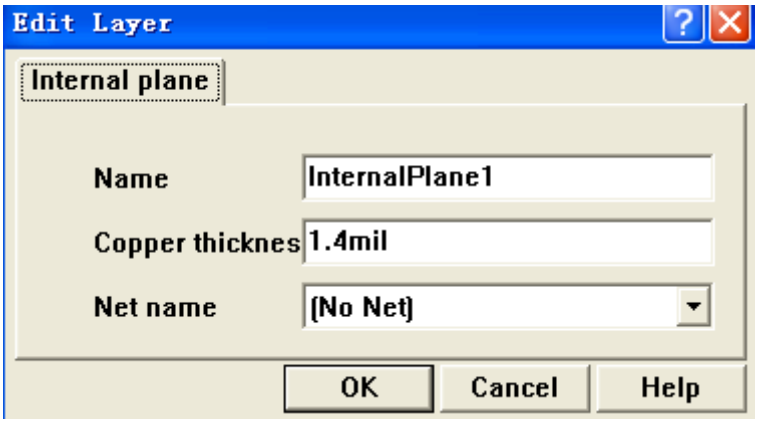
Copper thickness -- this value is required for signal integrity analysis



Plane Layers

Name -- User-defined layer name

Copper thickness -- this value is required for signal integrity analysis

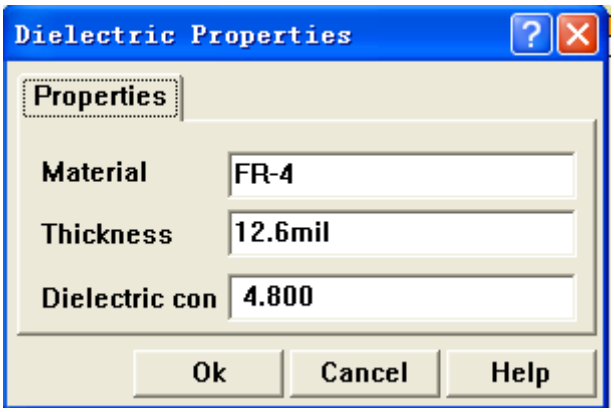


Substrate (dielectric) layers

Material -- material kind, this is entered for reference

Thickness -- the dielectric (substrate) thickness is required for signal integrity analysis

Dielectric constant -- dielectric constant of the substrate, required for signal integrity analysis.



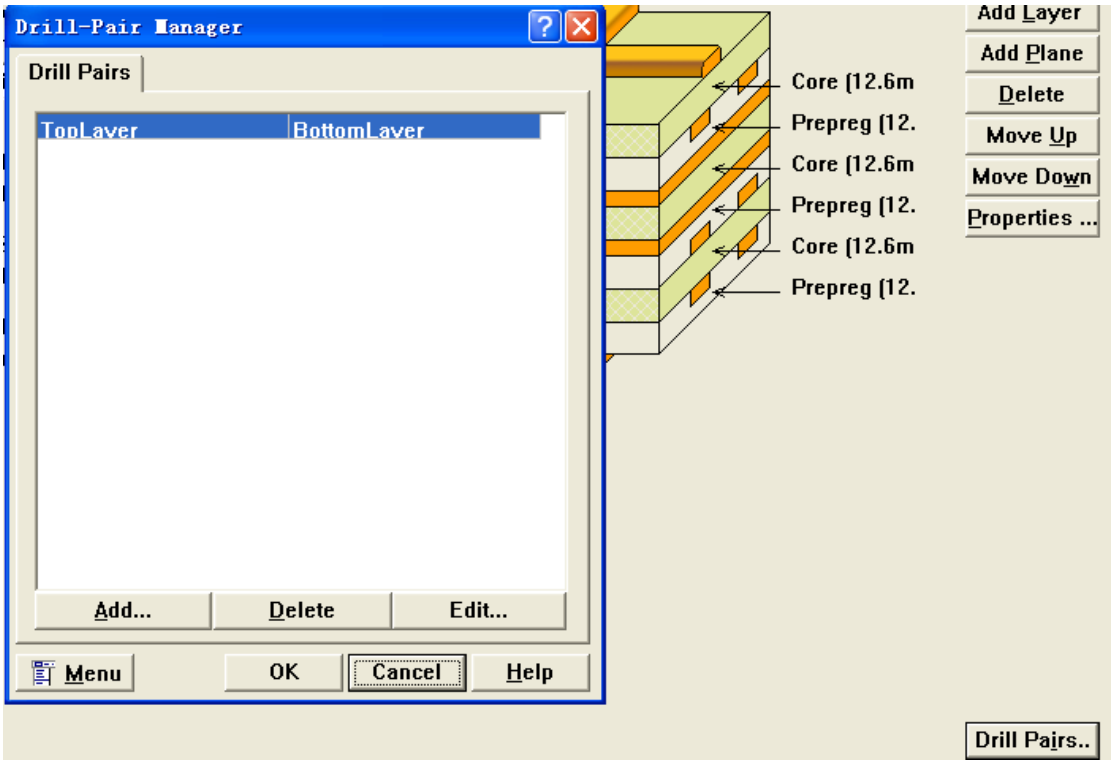
Defining the drill pairs

Part if defining the layer stack-up is to specify the drill-pairs. The term drill-pairs refers to the 2 layers that a drilling operation starts from, and stops at. Unless the board includes blind and buried vias only one drill-pair is required, comprising the Top and Bottom layers. This

drill-pair is on by default and can not be deleted or modified.

Drill-pairs are defined in the Drill-Pair Manager dialog, click on the Drill-Pairs button in the Layer Stack Manager dialog to display this dialog.

If the design includes blind and buried layers then the drill pairs must be defined to suit the layer stack-up style. This should be done in consultation with your board manufacturer to ensure that your design matches their fabrication technology.



Creating the mechanical definition of a PCB

The detail required for the mechanical definition of a board will depend on company and manufacturer requirements. Generally, manufacturers require board corner markers, a reference hole location and external dimensions as a minimum. Contact your PCB manufacturer for

details.

To create the mechanical definition of the PCB, you place tracks, dimensions and other PCB design objects on the four Mechanical layers available.

In general it is advisable to use one mechanical layer to draw the physical outline of the board, and then place dimensions, alignment markers, header information, etc. on the other mechanical layers.

It is good practice to design the physical board outline starting in the lower left region of the workspace. One inch in, one inch up from the absolute origin is often used as a position for the lower left corner of the board. The current origin can then be set as required.

Defining the PCB placement & routing outline

Before commencing the PCB layout process, you must create an electrical definition of your board. An electrical board definition involves the creation of a component placement and track routing outline for the board, as well as defining regions within this outline where placement and routing are excluded.

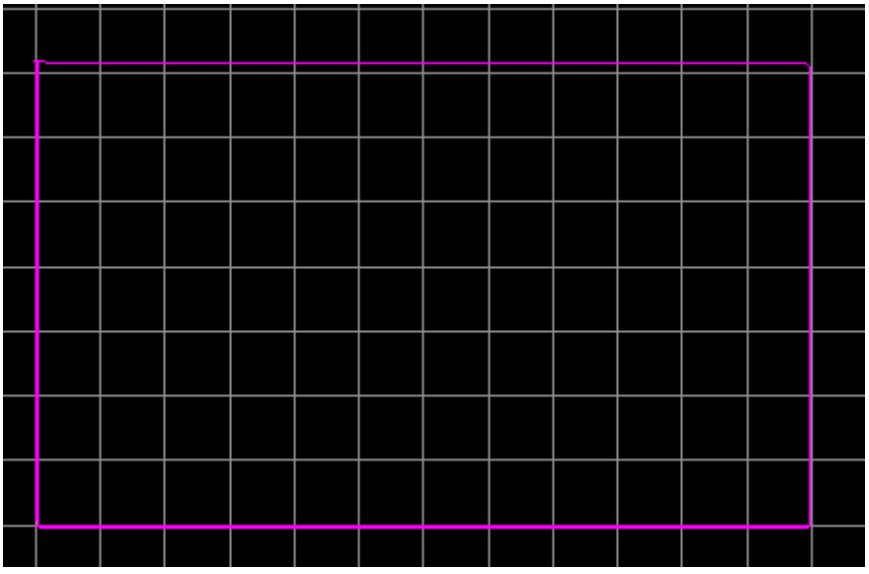
The placement and routing outer limits are defined by placing tracks and arcs on the Keep Out layer to define the electrical outline of the board. Typically this boundary is set slightly in from the physical edge of the board, ensuring that tracks and components do not get too close to the

edge. This boundary is used by the Design Rule Checker, the autoplacer and the autorouter to limit placement and routing within the boundary.

You can also define "no go" regions within this outline where components and/or tracks are to be excluded. This can include zones for mounting hardware and regions required for board profiling. These zones are created by placing design objects such as tracks, arcs and fills on the Keep Out layer, within the outer boundary.

The basic rule when using the Keep Out layer is that routing on signal layers will not cross over design objects on the Keep Out layer.

Keep out regions defined on the Keep Out Layer apply to all signal layers.



Using the Board Wizard to create a new PCB

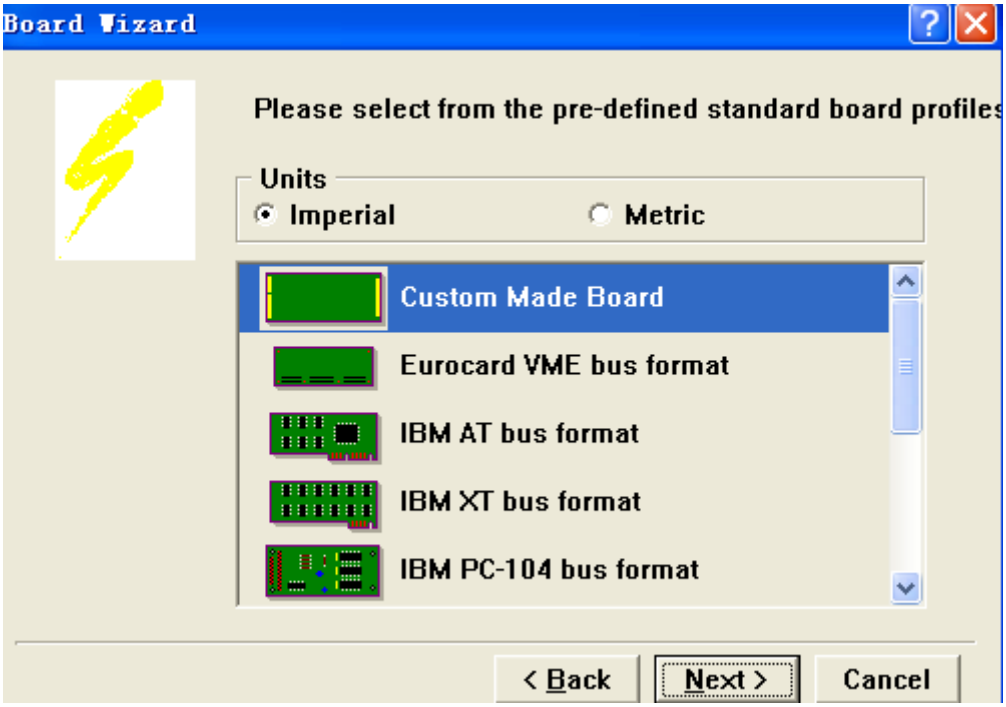
Protel 99 SE includes a Board Wizard (PCBMaker) which allows you to select from a large number of industry-standard board templates.

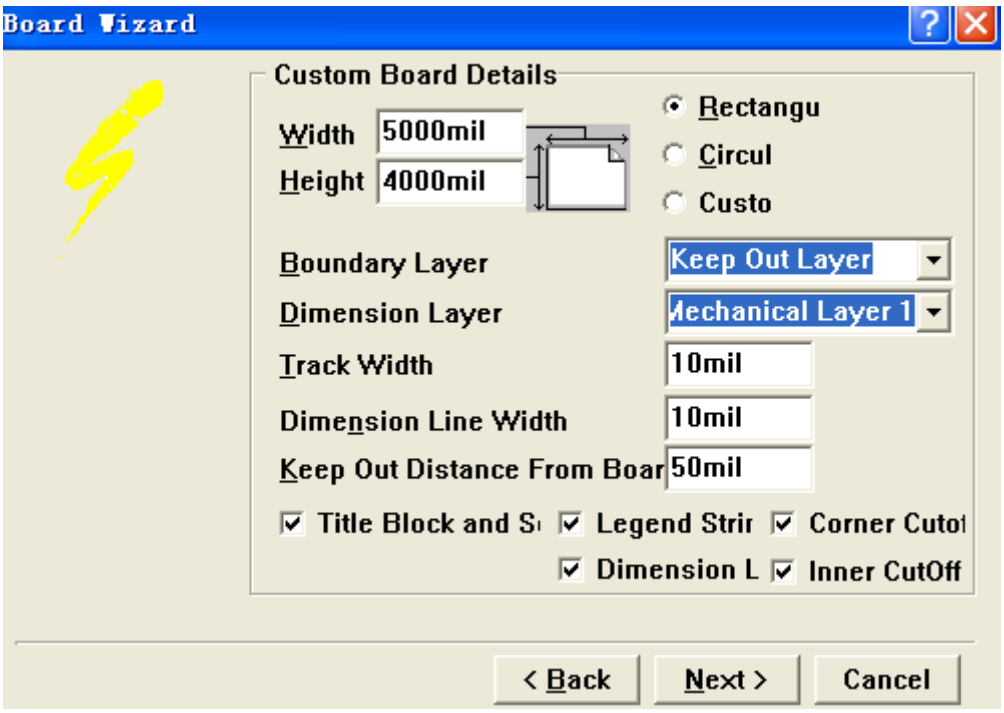
The templates include; a title block, alignment markers, reference rulers, dimensions, and standard edge connectors. The Wizard will fill the title block and let you to specify the number of routing layers and the track/pad technology.

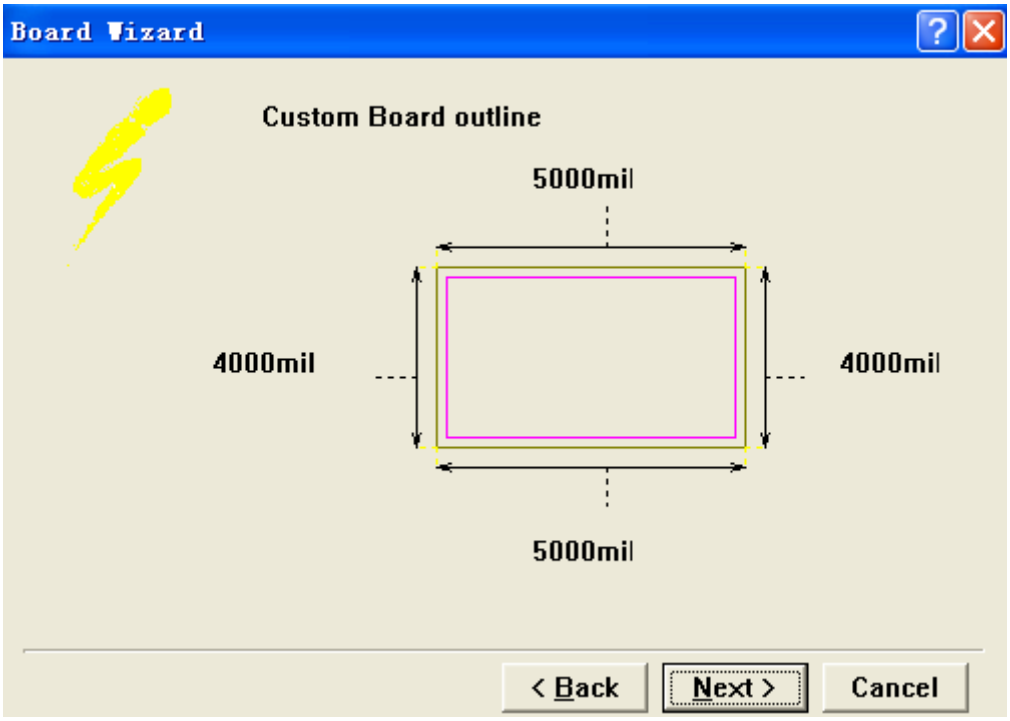
To create a new board using the board Wizard, select the File >New menu item. In the Wizards tab of the resulting dialog, select the PCBMaker icon and click OK. This will launch the Board Wizard which will guide you through the steps of creating a new board.

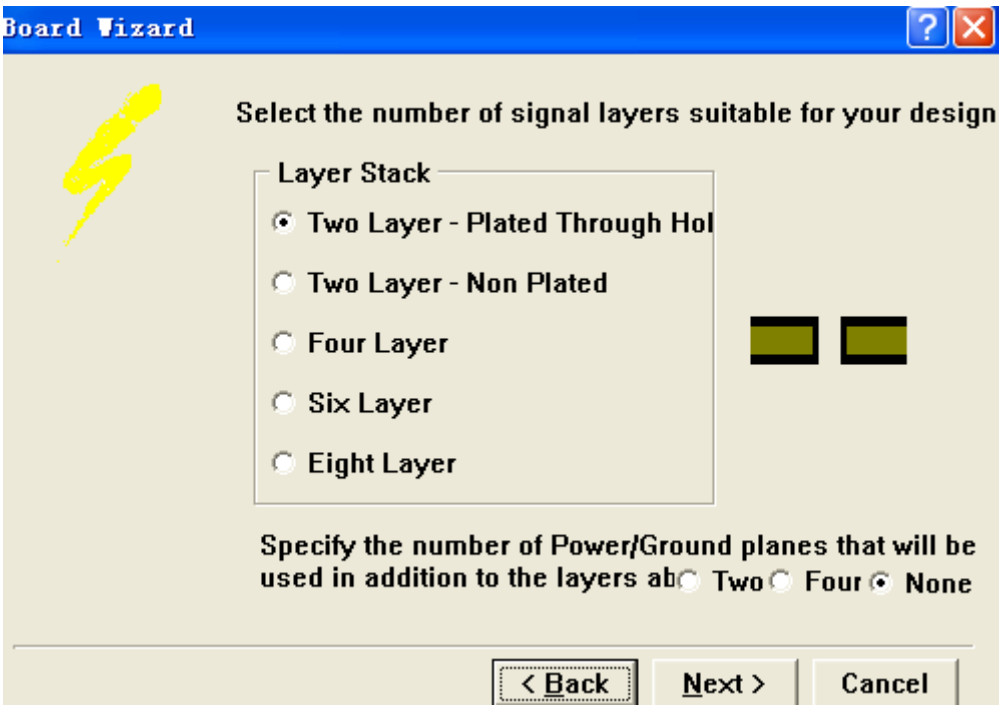
Select Custom Made Board from the board list in the Wizard to create a custom board outline. If you select this option, on the last page of the Wizard you have the option of saving the custom board as a new Wizard template. Enable this option and enter a name and description for the board template. The next time you run the Board Wizard, the new template will appear in the board list.

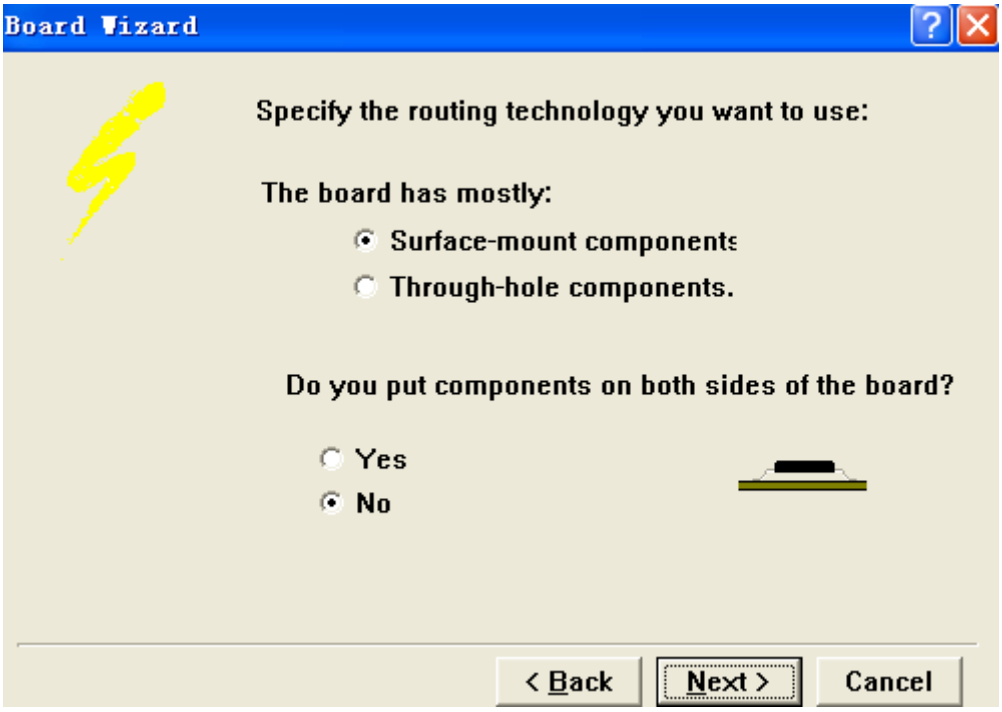

Board Wizard
Welcome To PCB Board Wizard
This wizard will help you create and set up a new printed circuit
board. It will take you through some simple steps to
< Back
Next >
Cancel

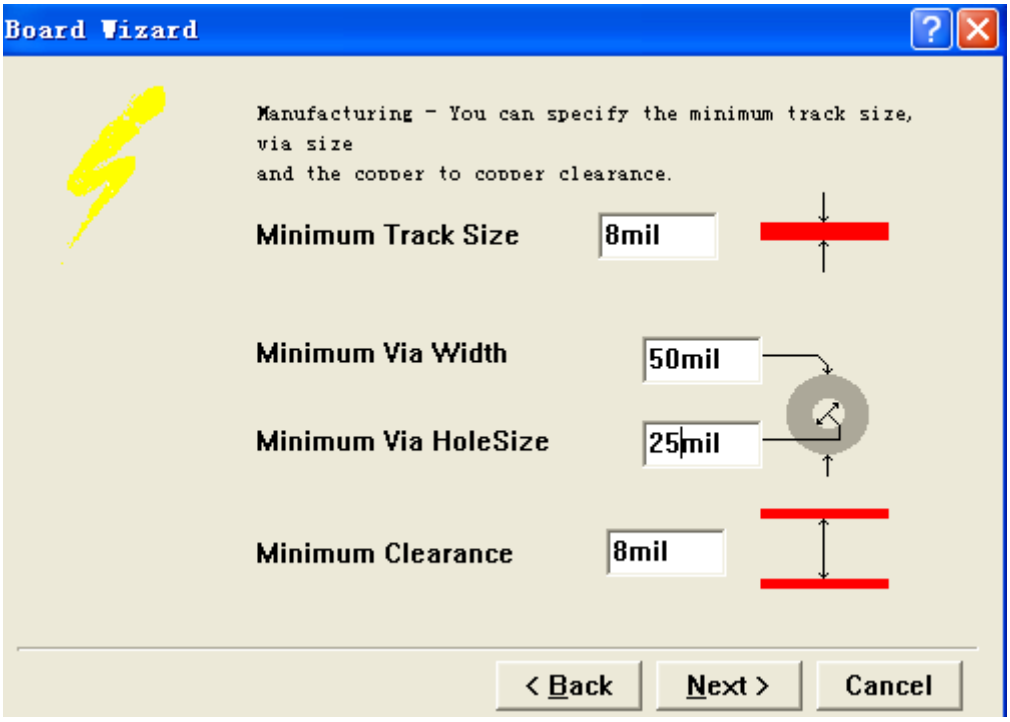

Board Wizard
Please select from the pre-defined standard board profiles
Units
Imperial
Metric
Custom Made Board
Eurocard VME bus format
IBM AT bus format
IBM XT bus format
IBM PC-104 bus format
< Back
Next >
Cancel


Board Wizard
Custom Board Details
Width 5000mil
Height 4000mil
Rectangu
Circul
Custo
Boundary Layer
Keep Out Layer
Dimension Layer
Mechanical Layer 1
Track Width
10mil
Dimension Line Width
10mil
Keep Out Distance From Boar
50mil
Title Block and S
Legend Strir
Corner Cutol
Dimension L
Inner CutOff
< Back
Next >
Cancel


Board Wizard
Custom Board outline
5000mil
4000mil
4000mil
5000mil
< Back
Next >
Cancel


Board Wizard
Select the number of signal layers suitable for your design
Layer Stack
Two Layer - Plated Through Hol
Two Layer - Non Plated
Four Layer
Six Layer
Eight Layer
Specify the number of Power/Ground planes that will be used in addition to the layers ab
Two
Four
None
< Back
Next >
Cancel


Board Wizard
Specify the routing technology you want to use:
The board has mostly:
Surface-mount components
Through-hole components.
Do you put components on both sides of the board?
Yes
No
< Back
Next >
Cancel



Loading a schematic design into a PCB document

In general a PCB design is not created from scratch, rather the design information is loaded into the PCB document from a schematic design. In Protel 99 SE this process if fully automated, with schematic information easily transferred into a PCB using Protel's "design synchronizer".

The synchronizer handles the initial transfer of information from the schematic to the PCB, as well as synchronizing subsequent design changes in both schematic and PCB documents.

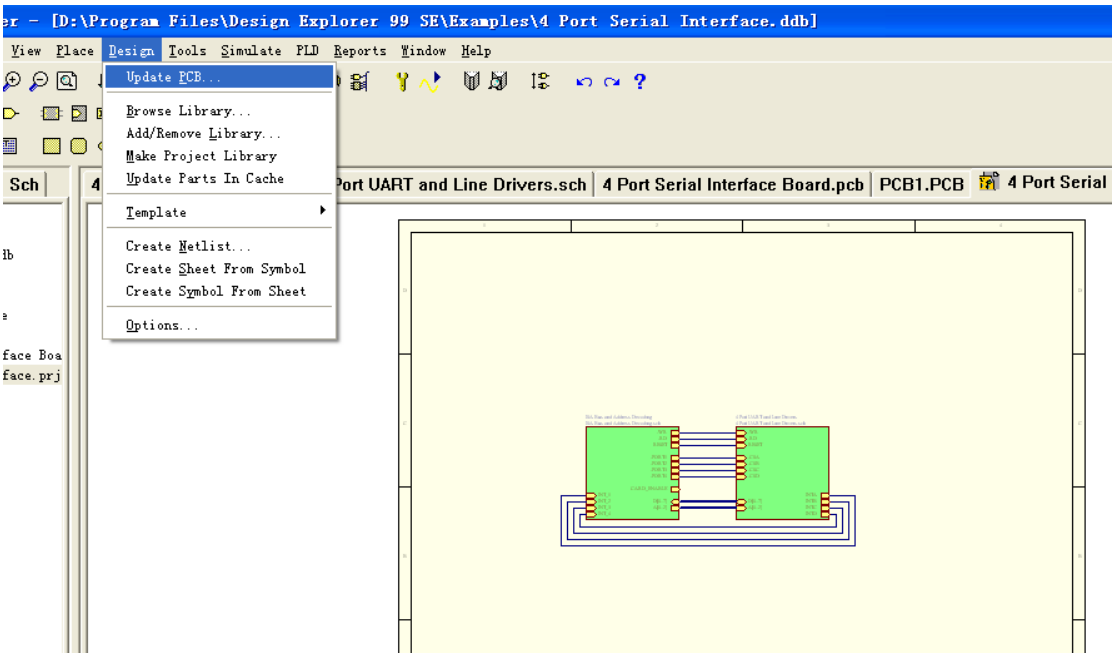
Before loading a schematic design into a PCB document, you should first define the mechanical and electrical outline of the board ,

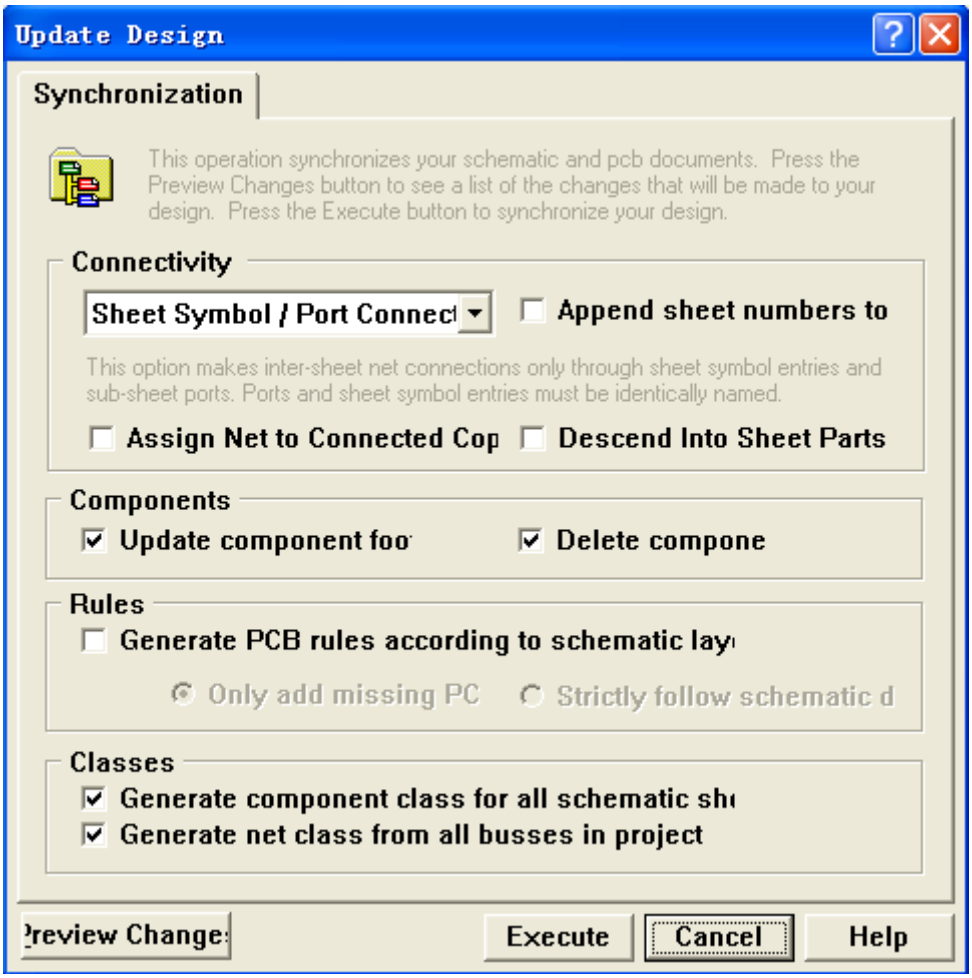
You should also ensure that your schematic contains all the

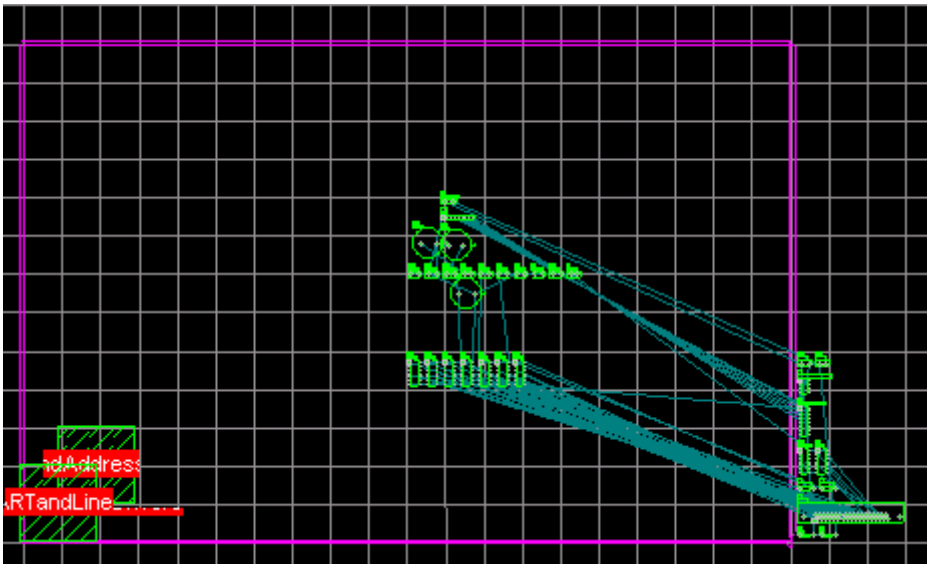
necessary information to successfully define the PCB

To load schematic information into a PCB document, from either the schematic or the PCB document select Design >Update PCB from the menus. For information on the running the synchronizer and updating subsequent design changes, see Synchronizing schematic & PCB documents in the links section below.

Once you have loaded a schematic design into a PCB document, all component footprints will be placed in the PCB design workspace ready for positioning, and all connectivity information will be displayed.




Update Design
Synchronization
This operation synchronizes your schematic and pcb documents. Press the Preview Changes button to see a list of the changes that will be made to your design. Press the Execute button to synchronize your design.
Connectivity
Sheet Symbol / Port Connec
Append sheet numbers to
This option makes inter-sheet net connections only through sheet symbol entries and sub-sheet ports. Ports and sheet symbol entries must be identically named.
Assign Net to Connected Cop
Descend Into Sheet Parts
Components
Update component foo
Delete compone
Rules
Generate PCB rules according to schematic lay
Only add missing PC
Strictly follow schematic d
Classes
Generate component class for all schematic sh
Generate net class from all busses in project
Preview Change
Execute
Cancel
Help

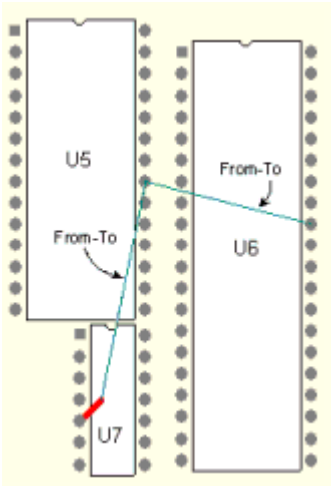


Part 4　PCB connectivity

When you load a schematic design into a PCB document, the pin-to-pin connections in each net are displayed as a series of thin connection lines. The line that connects each pin in the net to another pin in the net is called a From-To, going FROM one pin in the net TO another pin. The From-Tos are collectively referred to as the Ratsnest.

The pattern or arrangement of the From-Tos in a net is called the net topology. If a net has not been assigned a user-defined topology then From-Tos are arranged to give the shortest possible connection distances for the entire net, based on the current arrangement of the components.

If the net has a user-defined topology applied the connection line is added to maintain the topology, and is shown as a dotted line (called a Broken Net Marker), indicating that the net should be routed between these two points to maintain the topology.



specific topology can applied to a net by either defining a Topology Rule, or by defining fixed From-Tos in the Form-To editor.

Specifying PCB topology in the From-Tos editor

The arrangement or pattern of the pin-to-pin connections in a PCB is called the net topology. By default, the pin-to-pin connections of each net are arranged to give the shortest overall connection length (this topology is called Shortest).

To give you total control of the arrangement, or pattern of the pin-to-pin connections in a net, Protel allows you to define your own set of From-Tos. A From-To instructs the PCB editor to make a connection FROM this pin TO that pin.

To specify From-Tos for a net, from the PCB document select the Design >From-To Editor menu item to open the From-To Editor dialog. You can define one From-To for a net, a few From-Tos for a critical part of the net, or specify the entire topology of the net by defining From-Tos for all the pin-to-pin connections.

Use the Auto Generate buttons in the From-To Editor dialog box to quickly generate a set of From-Tos for the entire net with the selected topology.

If you create From-Tos for only part of a net, the remaining pin-to-pin connections will be set to the shortest topology.

The topology of a net may need to be redefined for a variety of reasons. High speed designs require that signal reflections must be

minimized. To achieve this the high speed nets are arranged with a daisy chain topology, where all the pins are connected one after the other, with the source pin at one end and a terminator pin at the other end of the chain. Another requirement of your design may be that all ground pins in the ground net connect back to a common point. A star topology could be applied to the ground net.

Display/hide connection lines in a PCB document

To make working with the ratsnest more manageable, you can selectively show and hide the pin-to-pin connection lines.

From a PCB document, select View >Connections from the menus to open the connection submenu [shortcut V C]. Select from one of the following menu items:

Show/Hide Net: Show/hide the entire set of pin-to-pin connections for the selected net. When you choose this option, a cross hair cursor appears. If you know the location of a pad on the net, click on that pad. If you do not, click in free space and a dialog will pop up, prompting for the net name. If you are unsure of the net name type ? and click OK to list all loaded nets.

Show/Hide Component Nets: Show/hide the entire set of pin-to-pin connections for all nets which connect to the selected component.

Show/Hide All: Show/hide all currently loaded (unrouted)

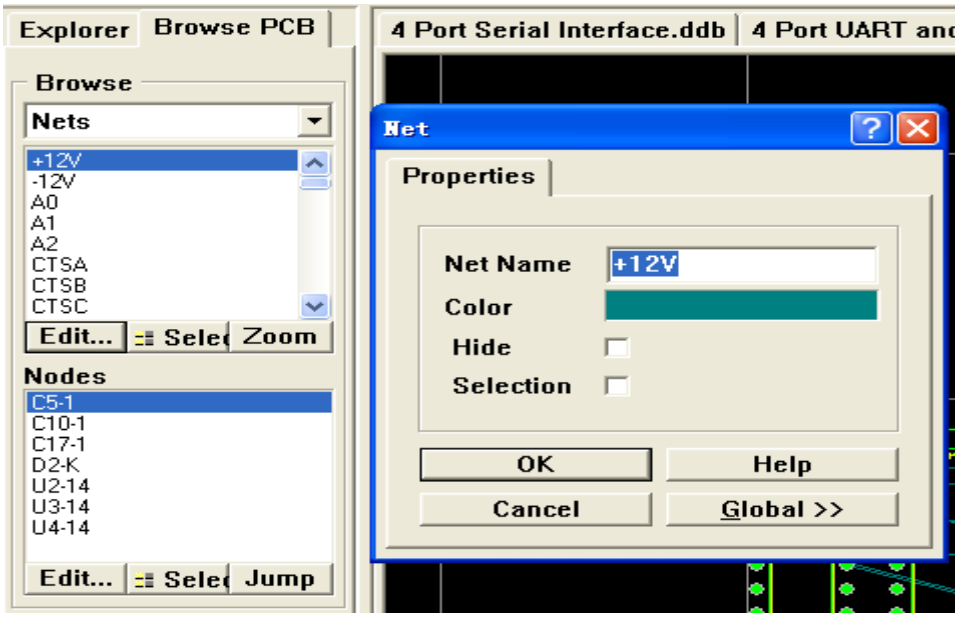
connections.

Note: During component moves all connection lines are automatically hidden, except those that go from a moving component to a non-moving component. The connection lines that are part of the move are automatically displayed. This behavior means that you can leave the connection lines set to hidden -any connection lines involved with a component move will automatically be displayed.

Changing the properties of a net in a PCB

Each net in a PCB design has a set of user-definable properties: net name; display color; and hidden status.

To edit the properties of a net, set the Browse mode of the PCB panel to Nets, select the net you want to change from the list, and press the Edit button. The Net properties dialog box will open.



In this dialog you can change the following properties:

Net Name: This field shows the current net name. Edit this field to change the name of the current net. Nets which are not defined by power objects or net labels, etc., in the source schematic will be given unique names of the form Nxxxxx. You can change the default names to something more appropriate.

Color: This field shows the color that the selected net will be drawn with in the ratsnest. Click on the color sample to change the display color of the net.

Hide: If this option is enabled, the selected net is not displayed in the ratsnest. If this option is disabled, the connections lines for the selected net will be shown.

Managing the netlist

Select Design >Netlist Manager from the PCB Editor menus to pop up the Netlist Manager dialog. There are a number of netlist management options available in the Menu button at the bottom of the dialog, including:

Modifying a net. Pins can be added and removed from a net, double click on the net name in the Nets in Class region of the dialog to display the Edit Net dialog. Use the transfer arrows to remove pins or add pins to this net.

Adding and deleting nets. Use the Add button at the bottom of the Nets in Class region of the dialog to add a new net, use the Remove button next to it to delete the currently selected net.

Add, remove and edit net classes. Use the buttons at the bottom of the Net Classes region of the dialog to add, remove or edit a net class. These operations do not change the netlist.

Exporting the internal netlist from the PCB. This option exports the current internal PCB netlist to a file.

Generating a netlist from the routed copper. This option creates a netlist file based on the connectivity created by the routing. It picks up a name for each net from one of the pads that the routing connects to.

Compare netlists. The netlist compare features can be used to compare the PCB netlist to an external netlist, or to compare 2 external netlist. Note that the same comparison can be achieved by selecting Design >Update PCB from the schematic editor menus, then clicking on the Preview Changes button at the bottom of the dialog. If there are no macros listed it means that the schematic and PCB netlists are matched.

Updating the net attributes of routing primitives from the net names on the component pads. This option is used to re-synchronize the net name of the routing primitives to the net name on the pads they connect to. Starting from each pad, the connected copper is selected and the net name of each primitive set to match the pad’s. Note that this operation

does not change the netlist.

Part 5 Managing PCB components

Protel 99 SE includes a comprehensive library of over 300 predefined through-hole and SMD component footprints for use in designing PCBs. Also, you can visit Protel's Web site for information on new and updated PCB libraries:www.protel.com

A "footprint" is the model of a component that is stored in a PCB library. When this footprint is placed in a PCB document, it is assigned a designator (and optional comment). It then is referred to as a PCB component.

Before you can use a footprint in a PCB design, the library containing the footprint must be available to the PCB editor.

Normally you do not need to manually add footprints to your design. When you load design information from a schematic into a PCB document, footprint information in the schematic is used to load all the necessary footprints into the PCB document.

To create or modify PCB footprints, you open the PCB library containing the footprint in the Design Explorer.

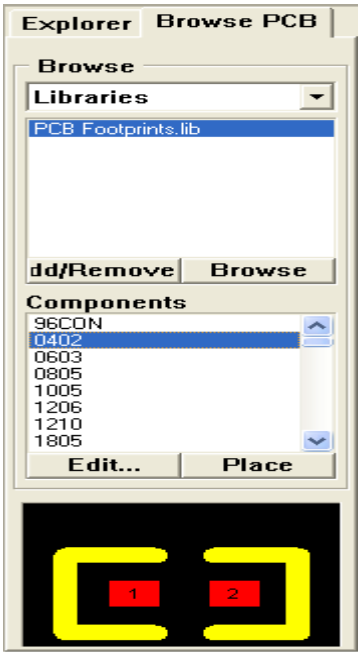
The footprint libraries supplied with Protel 99 SE are stored within design databases (.DDB files) in the Design Explorer 99 SE\Library\PCB

folder in your Protel installation directory.

Making PCB footprint libraries available for use

Before you can use a component footprint in a PCB document, you must add the library containing the footprint to the current library list in the PCB editor. In Protel 99 SE, PCB libraries can be stored in a design database, linked to a design database, or stored as separate files which have a .LIB extension. The footprint libraries supplied with Protel 99 SE are stored within design databases (.DDB files) in the Design Explorer 99 SE\Library\PCB folder in your Protel installation directory.

To view a list of current available libraries, with a PCB document active set the Browse mode on the PCB editor panel to Libraries. A list of all currently loaded libraries will appear in the top list box or the PCB panel. Click on a library in the list to display a list of the component footprints it contains in the lower list box. Clicking on a component will display a preview of the component footprint in the Mini Viewer at the bottom of the panel.



To add or remove libraries from the available libraries list, select

Design>Add/Remove Library from the menus, or press the Add/Remove button in the PCB editor panel to open the PCB Libraries dialog. Add or remove a design database from the list to add or remove all the PCB libraries it contains. Once all the libraries from that database have been added to the lower region of the dialog they can be selectively removed.

Once a library has been added, its name will appear in the Browse window of the PCB Panel, and footprints from that library can be used in your PCB document. The only limit to the number of libraries that can be available is the free memory on your computer.

Placing components from a PCB library

Normally you do not need to manually add footprints to your design. When you load design information from a schematic into a PCB document, footprint information in the schematic is used to load all the necessary footprints into the PCB document.

If you wish to manually add a component to the PCB document, you must first ensure that the PCB library containing the relevant foot print is loaded and available in the PCB editor .

To browse the components in an available library, from a PCB document set the Browse mode in the PCB editor panel to Libraries and click on the desired library in the list. When you click on a component in the Components list it will be displayed in the MiniViewer at the bottom

of the panel. To place the selected component, press the Place button (or double-click on the component name) in the panel.

To place a footprint directly from the PCB document, select Place >Component [shortcut P C] to open the Place Component dialog. Enter the component name in the Footprint field, or press the Browse button to search for a component in the loaded libraries. Set the Designator and Comment fields and click OK to place the component.

Editing the properties of a PCB component

To edit the properties of component placed in the PCB document, from a PCB document select Edit >Change from the menus and click on a component outline in the PCB document to open its Component properties dialog, or double-click within the component outline to open its properties dialog directly.

Properties tab

Set the designator and comment text for the component in the Designator and Comment fields respectively.

The Footprint field contains the name of the current footprint used for the component. The current component footprint can be changed to any other available footprint in any open library. When you type a different name in the Footprint field and click OK to exit the dialog, the PCB editor will

search the current open libraries and attempt to locate the new footprint. Component footprints can be changed freely. However, if there are netlist connections to the pads the new footprint must have the same used pin numbers available as the previous one. If it does not the warning message "cannot match pads with new footprint" will be displayed and the substitution will be aborted. For example, changing a DIP16 to an SMD16A is a legitimate change as the pin numbers match. Changing a DIP16 to a TO-3 would generate a warning and the change would be aborted. If the change is successful the connection lines will also be updated to remain connected to the appropriate pads.

The Layer field shows the current layer that the component is assigned to. Select a layer from the dropdown list to change the assigned layer.

Enable the Lock Prims options to lock the position of all primitives that make up the component relative to one another. If this option is disabled, you can change the shape of the component on the board.

Designator and Comment tabs

The options in the Designator and Comments tab are used to change the way the component designator and comment text is displayed

on the PCB document. You can change the size and font for the text, as well as the layer it appears on.

Enable the Hide option to hide the designator or comment text in the PCB document. Hidden text will not be printed or plotted.

Enable the Mirror option to have the text appear reversed.

Editing the shape of a placed PCB component

Generally, if a component footprint requires modification, the footprint is edited in the PCB library, and then the PCB is updated. This will update all instances of that footprint in all currently open designs. However, you can graphically modify the shape of an individual component on the board by unlocking the primitives that make up the component.

To do this, from a PCB document select Edit >Change from the menus or double-click within a component outline to open the component's properties dialog. In the Properties tab, uncheck the Lock Prims option and click OK to close the dialog.

The component primitives - the tracks, arcs, etc. that make up the footprint - can now be modified individually, allowing you to change the shape of the component.

To add new primitives to a component place the new primitives as required, select the new primitives (but not the existing component

primitives), then select **Tools →Convert →Add** Selected Primitives to Component from the menus. You will be prompted to click on the component that you want to add the selected primitives to. The target component must have its primitives unlocked to carry out this operation.

Even when a component's primitives are unlocked, the component is still recognized as a single component object in the PCB document. If you want to permanently convert a component into its constituent primitives, see the Converting a PCB component to its primitives topic in the links section below.

Converting a PCB component to its primitives

If necessary, a placed component can be converted back into its original set of primitive parts.

To PERMANENTLY ungroup a component, from a PCB document select the **Tools →Convert →UnGroup** Component menu item. When you launch this process you will be prompted "Select Component". Click on the component you wish to ungroup. The prompt "Confirm convert Component To Primitives" will be displayed. If you click YES (or press Y) the component designator and comment (if any) will be removed from the component, and the component will revert to the various primitives that it was made up from.

Creating a PCB project library

At any time in the PCB layout process, you can create a PCB footprint library that will contain all of component footprints currently placed in the PCB document. This library is called a project library.

To create a project library, from a PCB document select Design >Make Project Library from the menus. A new PCB footprint library will be created and saved in the design database in the folder that contains the source PCB document. All components in the current PCB document will be added to this library.

A PCB footprint library created in this way can be used as you would any other library.

Note: When it is created, the project library will be given a default name. You should change this name to one of your choice.

Re-annotating PCB component designators

Re-annotating component designators reassigns the component designators throughout the PCB design on a positional basis.

To re-annotate designators, from the PCB document select Tools >Re-Annotate from the menus to open the Positional Re-Annotate dialog. Select a re-annotation method using the option buttons in the dialog. As you select each method, a graphical description of the method is shown in the dialog.

Click the OK button to have all component designators on the board reassigned.

Note: If your PCB document is linked to a schematic, after a re-annotation you should select Design >Update Schematic from the menus to re-synchronize the schematic with the PCB.

Editing PCB footprint libraries

To be able to edit a PCB footprint library, the library must be stored in or linked to a Protel design database. The footprint libraries supplied with Protel 99 SE are stored within design databases (.DDB files) in the Design Explorer 99 SE\Library\PCB folder in your Protel installation directory.

To open a PCB library for editing, simply open the design database and double-click on the relevant library icon in the design window, or click on the icon in the navigation tree. This will open the library as a document in the Design Explorer and start the PCB library editor.

The PCB library editor includes a complete set of processes for creating, editing and placing library footprints. There is no limit to the number of component footprints that each library can hold.

Component footprints generally include one or more pads (corresponding to component pins and numbered accordingly) plus track and/or arc segments on the silkscreen (overlay) layer to define the

component body.

Note: When a PCB document is active, you can directly edit a component in an available PCB library by setting the Browse mode in the PCB editor panel to Libraries, selecting the library and component from the displayed lists, and clicking the Edit button on the panel. This will automatically open the design database containing the library and present the component for editing in the design window.

Opening a PCB library for editing

To be able to edit a PCB library in Protel 99 SE, it must be stored in or linked to a Protel design database.

To edit a PCB library, use the Design Explorer to open the design database containing the library or library link. Design databases that contain PCB libraries can be manipulated as you would any other design database.

Simply use the Design Explorer to open a stored or linked PCB library as a document within the design database. PCB library documents are automatically opened with the PCB library editor. The default PCB libraries supplied with Protel 99 SE are stored within a series of design databases located in the Design Explorer 99 SE\Library\PCB folder in your Protel installation directory.

Once a PCB is open, you can modify the components in the library, or

add or delete components.

Note: When a PCB document is active, you can directly edit a component in an available PCB library by setting the Browse mode in the PCB editor panel to Libraries, selecting the library and component from the displayed lists, and clicking the Edit button on the panel. This will automatically open the design database containing the library and present the component for editing in the design window.

Creating a new PCB Library

To create a new PCB library, first open or create a design database in which to store the library.

To create a new PCB library, from within a design database select File→New, and double click on the PCBLib icon in the New Document dialog. A new PCB library document will be created in the current folder of the design database. To open the library, double-click on its icon in the design window, or click on its icon in the navigation tree.

As a library is a set of component footprints, it can not exist without at least one defined footprint. When you create a new library, an empty component sheet (called PCBComponent_1) is also created within the library. To rename this default footprint, open the library, select PCBComponent_1 from the list in the PCB library editor panel, and select Tools >Rename Component from the menus.

1.Creating a new PCB component

To create a new component, you must first open the library that will hold the component (see Opening a PCB library for editing in the Links section below)

Once the desired PCB library file is open and active, select the Tools→New Component menu item. The Component Wizard will automatically start to guide you through the process of building a new PCB component.

If you do not want to use the Component Wizard, press Cancel to manually create a component. You will be presented with an empty component footprint workspace. Select Tools→Rename Component to give your new component a name (255 characters maximum).

Creating a component footprint uses the same tools and design objects that are used to design a PCB. Place tracks and arcs in the footprint sheet to create the body of the component, then place pads to form the component pin connections. As with PCB design, design objects can be placed on any layer. When you subsequently place the footprint on a PCB document, all objects that make up the footprint will be assigned to their defined layers.

2.Placing pads for a new PCB component

One of the most important procedures in creating a new component footprint is placing the pads that will be used to solder the component to

the PCB. These must be placed in exactly the right positions to correspond to the pins on the physical device.

To place a pad in a component footprint, when a footprint sheet is active in the design window, select Place ?Pad from the menus to call up a new pad.

Note: You should always build the component around the workspace 0,0 reference point. The reference is the point you will be "holding" the component by when you place it in a PCB document. Select Edit→Reference from the menus to open the Reference submenu. Select an option from this submenu to move the Reference if it needs to be changed. While a pad is "floating" on the cursor prior to placement, select Edit >Jump >Reference to position the cursor at the workspace 0, 0 coordinate. Prior to placing the first pad, press the TAB key to define the pads attributes.

Always build surface mount footprints on the top layer. Use the L shortcut key to flip them to the bottom layer during placement.

3.Drawing an outline for a new PCB component

Drawing a PCB footprint outline is done by placing tracks and arcs on the footprint sheet in the PCB library editor to form the body outline. Normally the footprint body is created on the Top Overlay layer so that it can be included in a silkscreen mask during manufacture of the PCB.

When placing tracks and arcs in a PCB footprint sheet the same

placement modes are available as for placing tracks in a PCB document to route the board.

The special strings .DESIGNATOR and .COMMENT can be added to the component in the PCB library editor if you require control over their layer, location and text attributes prior to placing the component. These will be displayed in addition to the standard designator and comment, which can be hidden if desired.

4.Including routing primitives in component footprints

Library components can also include routing primitives, such as tracks and arcs placed on signal layers.

If your components include routing primitives there is an option that automatically updates the net name of these primitives as the netlist is transferred from the schematic to the PCB. Enable the Assign Net to Connected Copper option in the Update Design dialog when you select Design→Update PCB from the Schematic Editor menus.

Net names can also be applied to routing primitives that are built into components at any time by selecting Design ?Netlist Manager from the PCB Editor menus. Select the Update Free Primitives from Component Pads option from the Menu button at the bottom of the dialog to reapply the pad net names to all connected copper.

5.Copying PCB footprints within libraries

Components can be copied and pasted between libraries, from a

library to a PCB, and from a PCB to a library.

To copy between libraries, or from the library to a PCB, select the component(s) in the Library Editor panel using the standard Windows selection keys (left-click, SHIFT+click and CTRL+click). Once the components have been selected click the right mouse button to pop up the floating menu and select Copy. Change to the target library, right-click in the Library Editor panel, and select Paste to add them to the target library.

If you are pasting directly onto a board select Edit→Paste from the PCB Editor menus.

6.Updating footprint changes in a PCB document

If you edit a component in a PCB footprint library and you want this change to be reflected in instances of the component placed on an existing PCB document, first open all PCB documents you wish to update as tabbed panes in the design window.

To update all instances of a component in all open PCB documents, from the footprint sheet in the PCB library editor, click the Update PCB button in the PCB library editor panel.

Validating component footprints

Use the Component Rule Check to validate all components in the current library. Select Reports ?Component Rule Check to pop up the Component Rule Check dialog. The Component Rule Checker tests for

duplicate primitives, missing pad designators, floating copper and inappropriate component reference.

Part 6 Using PCB design rules

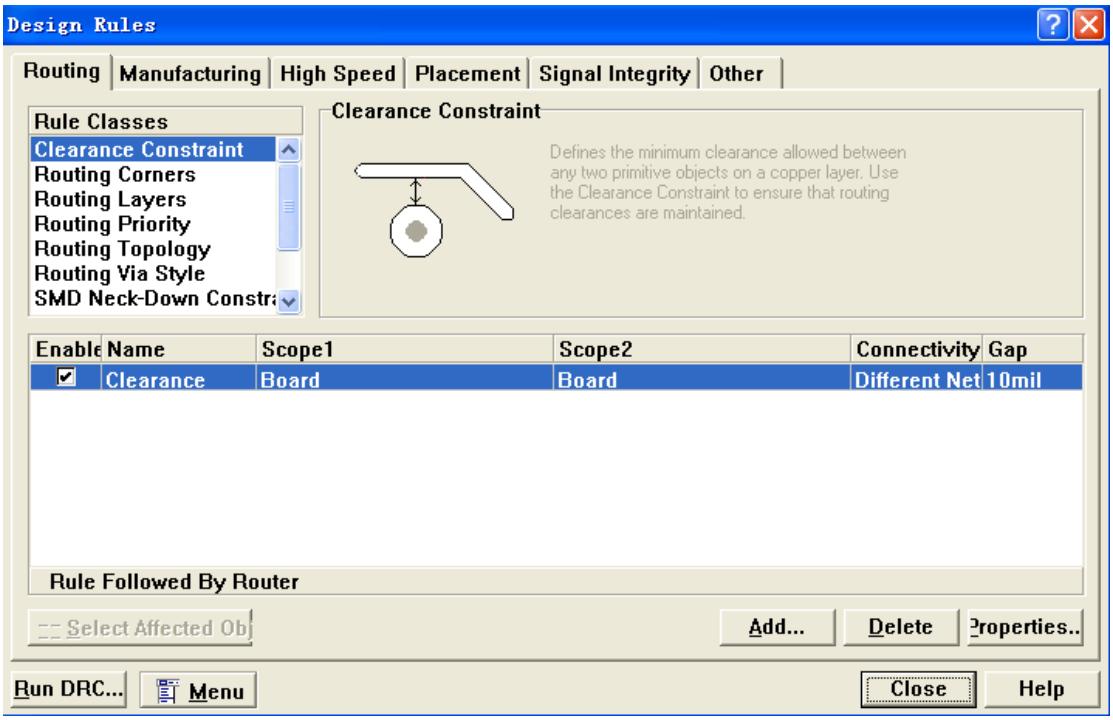
You design your PCB by placing components, tracks, vias and other design objects. These objects must be placed in the workspace with regard to each other. Components must not overlap, nets must not short, power nets must be kept clear of signal nets, etc.

To allow you to remain focused on the task of designing the board, Protel 99 SE can monitor these design requirements for you. You instruct the PCB editor of your requirements by setting up a series of design rules. These design rules are monitored as you layout the PCB. As soon as an object is placed in violation of a design rule it is highlighted. Also, during the board verification process you can run the integrated Design Rule Checker, which will generate a report of any design rule violations in you PCB.

Protel allows a wide range of design rules to be defined for a PCB. These include clearances, object geometry, parallelism, impedance control, routing priority and topology, placement rules, and signal integrity rules. Each rule has a Rule Scope that defines how it is applied.

The scope allows you to apply a rule to objects, nets, net classes, components, component classes, layers, regions, through to the whole board.

Design rules are set up and configured in the Design Rules dialog box (from the PCB document select Design >Rules).



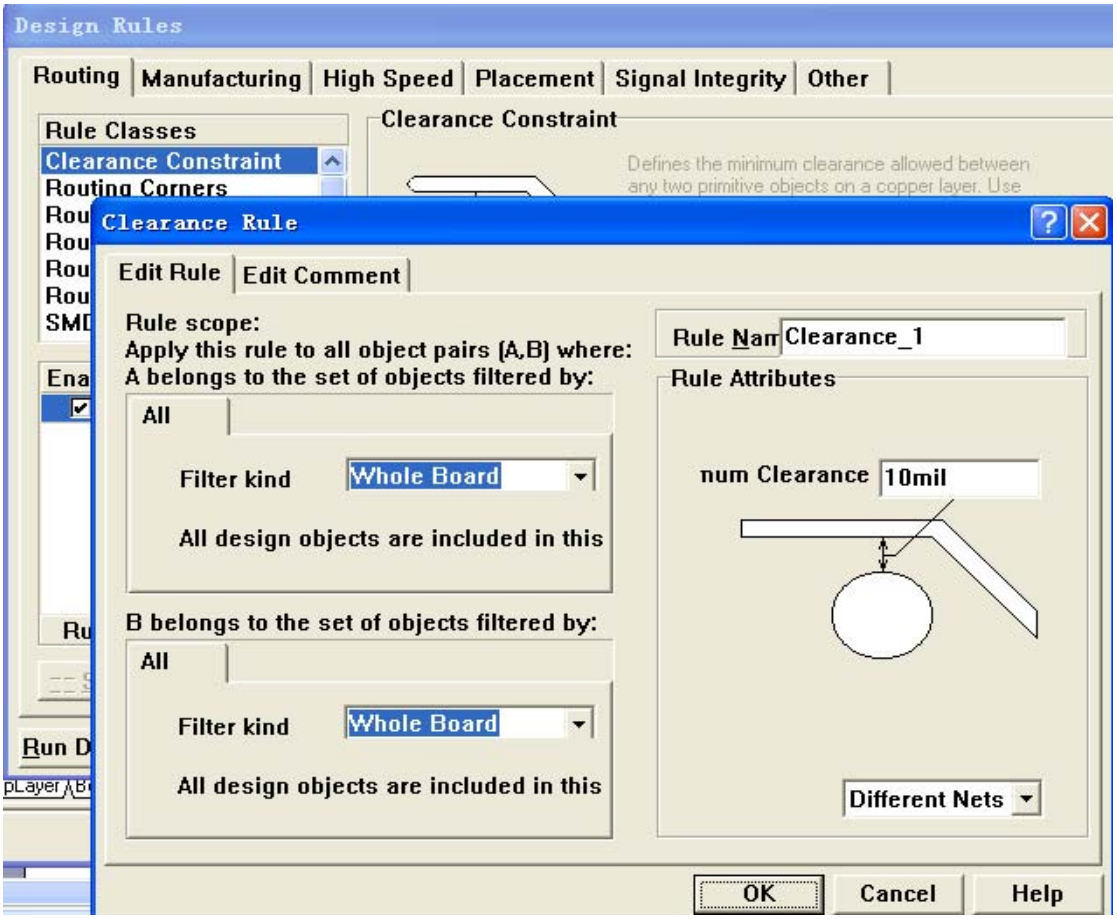
Creating and editing PCB design rules

To create a new design rule for a PCB layout, from the PCB document select Design >Rules to open the Design Rules dialog.

This dialog contains a series of tabs representing different classes of design rules. Each tab contains a Rule Classes box that lists the specific design rules available from that tab. Select the appropriate tab.

From the Rule Classes list, select the type of rule you wish to create

or edit. A list of all rules of that type currently active will appear in the rules list box. Select a rule from the list and click the Properties button (or double-click on the rule in the list) to edit that rule.



Click the Add button to add a new rule of the selected type. The properties dialog for that rule type will open. Set the various options for the rule, define the Rule Scope, and click OK to create the rule. It will appear in the rules list.

Rules can be disabled in the Design Rules dialog. Disabling a rule has the same effect as deleting the rule in terms of how it is handled by the on-line and batch DRC.

Note: A list of currently defined rules can be displayed in the PCB

panel, set the Browse mode to Rules.

Setting the scope of a PCB design rule

The scope, or extent of each Rule is determined by the Rule Scope. The scope allows you to define the set of target objects that a particular instance of a rule is to be applied to. You set the rule scope in the rule's properties dialog when you create or edit the rule.

By setting the scope you could apply a rule to the whole board, or you could target a particular net, component or pad. Protel 99 SE also allows you to set a compound scope for any design rule, which allows you to specifically target particular design objects. See the Compound design rule scope topic in the Links section below for information on this.

Another way to target specific groups of objects is to create object "classes" and then set the scope to target a class. See the Creating classes of PCB objects topic for information on this.

For example, your design might include mains level voltages requiring a clearance of 100 mils, and logic level voltages requiring a clearance of 10 mils. These requirements can be achieved by defining two copper clearance rules, one with a scope of net class (the net class would include the mains level voltage nets) and a clearance of 100 mils, the other rule with a scope of board and the clearance set to 10 mils.

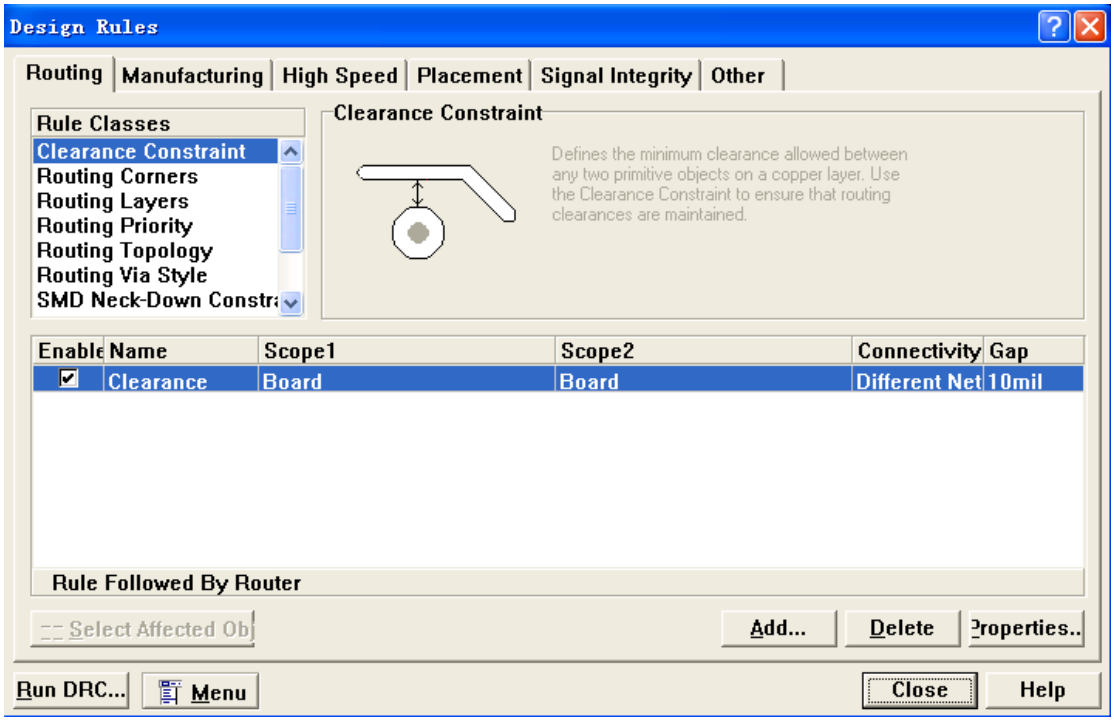
There are two types of design rules, unary rules and binary rules. Unary rules apply to one object, or each object in a set of objects. Binary rules apply between two objects, or between any object in one set to any object in the second set.

An example of a unary rule is the solder mask expansion rule. This rule applies individually to each pad identified by the rule scope. An example of a binary rule is copper clearances, which applies between any copper object in the first set and any copper object in the second set, as identified by the two rule scopes. When you configure a unary rule you setup one rule scope, when you configure a binary rule you setup two rule scopes.

PCB design rule definitions

Protel 99 SE allows you to create design rules in a number of different areas.

To create or edit a design rule, from the PCB document select **Design→Rules** to open the Design Rules dialog. Select the tab for the appropriate rule class, and select a rule type from the Rule Classes list. Click the Add button to a add a new rule of the selected type. Select an existing rule in the rules list and click the Properties button to edit the rule.



Importing and exporting design rules

Rule sets can be exported and imported, allowing you to store and retrieve favorite rule sets. To import or export a rule set click on the Menu button at the bottom of the Design Rules dialog. When importing rules you can either Overwrite or Add them by clicking the appropriate button in the rule Import Options dialog. Overwrite occurs when a rule with the same rule name is encountered.

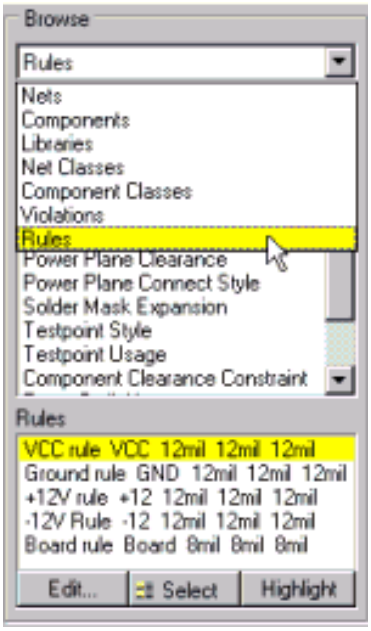
Part 7 Navigating a PCB document

When a PCB document is active, the View menu includes a range of

options for controlling the view of the main document window. Each view option has defined menu shortcut keys. You can use these shortcut keys to change views, even when another process (such as placing an object) is active.

- View→Fit Document: Changes the view to display all objects in the workspace.
- View→Fit Board: Changes the view to display the entire board, based on the board keep out boundary.
- View→Area: Redefines the display area. Click to define the first corner, then drag the dotted zoom window to define the new display area.
- View→Around Point: Redefines the display area. Click to define the center point, then drag the dotted zoom window to define the new display area.
- View→?Zoom In: Brings the design closer to you, relative to the cursor position on the board.
- View→Zoom Out: Moves the design away from you . This is also relative to the cursor, so position the cursor first. To zoom in and out in smaller increments hold the SHIFT key while pressing PAGEUP or PAGEDOWN.
- View→Zoom Last: Returns you to your last view of the screen . Repeatedly pressing V L allows you to toggle back and forth

between two views.



When a PCB document is active, the PCB editor panel can be used to browse the various objects on the current PCB document.You can set the Browse mode to either Nets, Components, Net Classes, Component Classes, Violations or Rules. If you browse by Net or Component the small MiniViewer in the panel will display the selected net or component. Use the Zoom button to quickly locate and identify the selected net or component in the main document window.

When an item in the panel is selected, information about that item will appear on the Status Bar. Press the Edit button to edit the properties of the selected object. Press the Jump or Zoom button to have the selected object centered in the document window. Press the Select button to select the chosen object in the workspace.

The message zones on the Status Bar can be resized -- position the cursor over an arrow symbol on the status bar, when the cursor changes to a double-headed arrow click and drag to resize a message zone.

Part 8 Manually routing a PCB

Routing is the process of connecting the various components of your PCB design with tracks and arcs. Because Protel's PCB editor automatically monitors net connectivity for you, manual routing is very straightforward. You place tracks, vias, fills and arcs to create the physical connectivity, and the software monitors the connectivity and updates the connection lines accordingly.

To begin manual routing of the board, simply select Place→Interactive Routing from the menus and start placing a track to route a connection.

If you place a track on a design object that has a net name, the track you are placing will adopt the net name, becoming part of that net. If you click on a connection line, the cursor will jump to the nearest pad, and then keep the connection line attached to the end of the track you are placing. If you click on a pad that has multiple connection lines one is automatically selected, ready for routing. Press the CTRL+SPACEBAR shortcut to cycle through each of the connection lines coming from this pad.

Because the connectivity analyzer automatically monitors the completion status of any net you are routing , you can route without regard to the arrangement of the From-Tos. Once you complete a connection, the entire net is reanalyzed and connection lines are added

and re-optimized as necessary.

Part 9 Autorouting a PCB

Protel 99 SE provides an easy to use, powerful, high-quality, shape-based autorouter, tightly integrated with the PCB design editor. When you run the autorouter, the board is routed directly in the PCB window, and adheres to relevant design rules set for the board.

In general, the autorouter does not need the set up of any options, as it will analyze the current PCB design and automatically select the most appropriate autorouting strategy. It is important, however, to ensure that any relevant design rules are set up prior to running the autorouter.

If you have pre-routed any connections on the board, ensure that the Lock All Preroutes option is enabled in the Autorouter setup dialog before running the autorouter.

To start autorouting the active PCB document, select **Tools→Auto Route→All** from the menus.

Preparing a PCB document for autorouting

When designing and setting up a board for autorouting, keep in mind the following important points:

- The board must include a closed boundary on the keep out layer.

- Objects placed on the keep out layer create blocks for the router on all layers.
- Signal layer objects with no net name create blocks for the router on that signal layer.
- Objects on the mechanical layer are not considered by the router.

Setting up the autorouting design rules

The autorouter obeys the relevant design rules setup for your PCB document. You should ensure that these design rules are configured correctly for your design before running the autorouter.

PCB design rules are defined by selecting **Design→Rules** from the menus when the PCB document is active. The Design Rules dialog includes a status line that reports whether the currently selected rule definition is followed by the router.

Protecting pre-routes before autorouting

Often you will want to manually pre-route certain nets, then autoroute the remainder of the board. You can protect the pre-routes from being ripped up and re-routed by the Autorouter by enabling the Lock All Preroutes option in the Autorouter.

When this option is enabled all pre-routes, including partially routed connections and nets, will be locked by the autorouter before routing.

When this option is disabled, the autorouter will rip up any pre-routed track segments which do not have their Locked option set.

Running the autorouter

To run the autorouter, from the PCB document select Tools ?Auto Route from the menus, and select from one of the following options:

- Autoroute All: Routes the entire board with the current routing setup.
- Autoroute Connection: Select this option and click on a connection to route that individual connection. Not all of the Autorouter algorithms are used in this made, so this method is not recommended for routing an entire board.
- Autoroute Net: Select this option and click on any connection line in the net. All connections in the net will be routed, using all the routing passes.
- Autoroute Component: Select this option and click on a component and all connections starting/ending on that component will be routed. Note that within a net, only the connections starting and ending on the selected component will be routed, using all routing passes.
- Autoroute Area: Select this option and click-and-drag the mouse to define the area to be routed. All connections starting and ending

in the designated area will be routed, using all routing passes.

While the autorouter is running, you can open the Auto Route menu and select one of the following options:

- Pause: You can Pause the autorouter at any stage during the autorouting process. Select Re-start to continue routing.
- Restart: Restarts the router after pausing.
- Reset: Resets the autorouter.
- Stop: Ends the autorouting process. Any completed routing on the board will be retained.

Part 10 Verifying the PCB design

Design verification is the process of investigating the PCB design for errors or potential problems before proceeding to manufacturing.

Protel is a rules-driven PCB layout environment and includes comprehensive design rule checking. Many of the design rules can be monitored and enforced on-line as you work, helping to prevent design rule violations during placement and routing. You can also manually run a design rule check (DRC) in batch mode at any time in the design process to check for conformance to specific rules.

To help solve signal integrity rule violations, Protel 99 SE includes a powerful Signal Integrity Analyzer that allows you to perform reflection and crosstalk simulations on your PCB.

You can also generate a number of reports that provide detailed information about your board design.

Setting up & running the PCB Design Rule Checker (DRC)

Protel 99 SE includes a powerful Design Rule Check (DRC) feature that verifies that the design meets the requirements specified by the design rules. It tests for routing violations such as clearance errors, unrouted nets, width errors, length errors and also conditions that effect manufacturing and signal integrity.

The DRC can be set to run in the background as you work, flagging and/or automatically preventing design rule violations. This mode if operation is known as the Online DRC. For information on setting up this feature, see the Setting up the PCB Online DRC topic in the Links section below.

You can also manually run the DRC at any time during the board design process to check for violations to specific rules. This mode of operation is known as batch-mode DRC.

To run the DRC in batch mode, from the PCB document select *Tools >Design Rule Check* from the menus to open the Design Rule Check

dialog. In the Report tab enable the rules that you wish to check and set the other options as appropriate. Click the Run DRC button to start the batch-mode DRC. Once the check is complete the report file will be opened in the design window listing any rule violations.

Checking the signal integrity of a PCB

As PCB designs become more sophisticated, with higher clock speeds, higher device switching speeds, and higher density, the need to analyze the signal integrity before the design is manufactured becomes more pressing.

Protel99 includes a sophisticated Signal Integrity Simulator, which can analyze the PCB layout and check that it functions within the design parameters, testing such things as overshoot, undershoot and impedance requirements.

The Signal Integrity Simulator uses the characteristic impedance of the traces, calculated through a transmission line calculator, and I/O buffer macro-model information, as input for the simulations. It is based on a Fast Reflection and Crosstalk Simulator which produces very accurate simulations, using industry-proven algorithms.

If the board fails any of the signal integrity design requirements (specified as design rules), you can then run a reflection or crosstalk analysis from the PCB, to see exactly how it is behaving.

If the design does not include a power plane, the analysis will still be performed, but the results can not be considered accurate.

Generating PCB analysis reports

There are number of reporting features that help analyze the board during the design process. These reporting features are launched from the items in the Reports menu.

Part 11 3 dimensional PCB visualization

The 3D PCB Viewer is a visualization tool that allows you to preview and print a 3D image of your PCB. The 3D Viewer is built around an OpenGL-based rendering engine, a standard graphics language supported by most graphics cards. It uses a run-time component modeling algorithm that uses the component designator prefix, footprint and outline shape to automatically select model and texture information and construct a suitable component model. Components that can not be recognized are automatically extruded.

To create a 3 dimensional view of your board select **View→Board in 3D** from the menus. The board is analyzed and a 3D view is created in a new Window.

Changing the View of the Board

The 3D Viewer supports full rotational and zoom control, making it possible to display the board at any angle. The board can be rotated by clicking-and-dragging in the MiniViewer window in the panel. The standard PCB Editor display shortcuts are also supported -- press the PAGEUP and PAGEDOWN keys to zoom in, the END key to redraw the view, right-click and drag on the 3D image to display the slider hand and slide the 3D view around.

You can also selectively hide the components, silkscreen outlines, copper, and text strings. These options can be enabled in the panel, or the 3D Viewer **Preferences** dialog.

The Browse PCB 3D panel also includes a highlight feature, click on a net name and click the Highlight button to highlight that net on the board. There is also an Animate option, which flashes the net that is being highlighted. The highlight color and the animate feature are set up in the **Preferences** dialog.

Printing the 3D View

The 3D view can be printed by selecting **File→Prin**t from the 3D Viewer menus. This will print what is currently displayed in the 3D window. Three print qualities are supported, Draft, Normal and Proof. The print quality is selected in the **Preferences** dialog (select **View**

→**Preferences**).

Part 12 Printing to a windows printing device

An essential part of the design process is producing printed documentation about the PCB design. This could include a manufacturing drawing detailing the fabrication information, check plots for verifying the contents of each fabrication layer, and assembly drawings detailing component location information and loading order.

In Protel 99 SE printed output is created by preparing a preview of the required printouts, then printing them from the Print/Preview window. Using this approach you can define precisely what mix of PCB layers you want to print, set the scaling and orientation, and see exactly how it will look on the page before you print it.

Protel 99 SE's print engine also supports printing the current screen area, and copying the current preview to the Windows clipboard, making it easy to include PCB information in your documentation.

The Print/Preview feature works by creating a Power Print Configuration document (*.PPC). This PPC document details: which PCB is being previewed, the target printer, the set of printouts, and the PCB layers to include on each printout. When you open a PPC document

this setup information is read, the PCB is analyzed, and the previews of the PCB are displayed in a separate Tab in the database window. You can then print the printouts as required.

Because the actual PCB data is not stored in the PPC document it must be extracted from the PCB when you create, modify, or open a PPC document. This analysis happened automatically -- if you prefer you can disable automatic rebuilding in the Preferences dialog and then use the Rebuild button (when you change the preview configuration), or Process PCB button (when you modify the PCB) in the Browse PCBPrint panel to update the previews.

Unit 7 Synchronizing schematic & PCB documents

Protel99 includes a powerful design synchronization tool, that makes it very easy to transfer design information from the schematic to the PCB (and back again).

The Synchronizer will automatically extract the component and connectivity information from the schematic, locate the required footprints in the PCB libraries and place them in the PCB workspace, then add the connection lines between connected component pins.

You use the synchronizer to initially transfer your design from the schematic documents to a PCB design document, and also to synchronize design changes made in either the PCB or the schematic documents.

Before you transfer the design information from the schematic into the new PCB outline, you must make the appropriate PCB footprint libraries available to the PCB editor. When you add a PCB library to the available library list, the footprints in that library can be placed in the PCB workspace.

There are several synchronization option that you can set to control the way the synchronizer behaves. To set these options, from a schematic

or PCB document select Design→Synchronization Options from the menus. The following options can be set:

- Connectivity Generation: This options specifies how the inter-sheet connectivity is created in a multi-sheet schematic. The Net Identifier Scope must be set to match the type of electrical hierarchy you have used when creating the multisheet schematic design. If the design has changed so that the net names on the routing no longer match the net names on the PCB component pads, enable the Assign Net to Connected Copper option to automatically reapply the pad net names to all the connected routing.
- Rules Generation: Enable the Generate PCB Rules option to have the Synchronizer create design rules from PCB Layout directives in the schematic. Click on option button select the rule creation mode. Only add missing PCB rules creates a new rule from a PCB Layout directive if there is no rule already defined for this net, existing rules are updated to match the settings in the PCB Layout directive. Strictly follow Schematic directives mode creates a new if there is no rule defined for this net, and existing rules are updated to match the settings in the PCB Layout directive. Any existing net scope rules of the relevant type are removed.
- Component Classes: Enable the Generate Component Classes and

Placement Rooms option to have the synchronizer create a PCB component class from each schematic sheet. Each component class is given the same name as the schematic sheet it is created from, with any spaces removed. Multipart components that span more than one sheet are included in the class of the sheet that contains the first part of the component. A PCB placement room is also created for each component class. These placement rooms are spread across the board, ready for positioning.

- Net Classes: Enable the Generate Net Classes for all Buses in Project option to create a PCB net class for each schematic bus.

If there are any PCB Layout directives placed in the source schematics, the synchronizer will translate these into PCB Design Rules. The settings in each Layout directive are translated into appropriate design rules, with a Rule Scope of Net.

When you run the synchronizer it first attempts to locate the target document. It uses the following approach to Indentifying the target document.

It looks for a target PCB in the same folder in the design database as the schematic project. If it finds a PCB it uses this. If there is more than one PCB in this folder the Synchronizer dialog appears, prompting you to select the correct one. If there are no PCBs in the same folder, the entire design database is searched, and you are prompted to select the correct

PCB from a list of all the PCBs in the design database. If there are none in the design database a new PCB is created, in the same folder as the schematic project.

To transfer the design information from the schematic to the PCB, the synchronizer extracts the component and connectivity information and creates a set of macros. Each action that is has to perform, such as adding a new component, adding a new net, or adding a node to a net, is defined by a macro.

If any macro can not be carried out (for example there is no footprint available), it is flagged as an error in the Changes Tab of the Update dialog. Prior to executing the Macros it is good practice to resolve any errors. Press the Reports button at the bottom of the Changes Tab for a complete description of all the macros.

When a schematic and its PCB have been synchronized, matching schematic and PCB components are assigned a matching identifier. This approach means that you are free to separately re-annotate the schematic or the PCB. They can be bought back into harmony at any time by running an Update from the design menu.

If a component without a matching identifier is found in either the schematic or the PCB, the synchronizer attempts to find a matching component for it. These matches are shown in the Confirm Component Associations dialog, which automatically appears whenever unmatched

components are detected by the synchronizer.

The synchronizer does this initial match by designator, always check that the matches are correct. When you click on the Apply button the matched components will be given a matching ID.

In Protel 99 SE, when a PCB document is synchronized with its source schematics, special synchronization specific information is stored as part of the PCB and schematic document formats. When you import into a Protel 99 SE design database a PCB design and associated source schematic project that was created with an earlier version of Protel design tools, you should run the Protel 99 SE Synchronizer to synchronizer to update both the PCB and schematic documents with this information.

To do this you must either update the PCB from the schematic, or update the schematic from the PCB. The method you choose should be determined by considering which of the imported documents (the PCB or the schematic) contains the most up-to-date design information. If you have added components, changed footprints, etc. on the PCB, and these changes are not yet reflected in the schematic, then you should update the schematic from the PCB. If, however, there are circuit changes, changes to parts, etc. in the schematic that have not been reflected in the PCB design, then update the PCB from the schematic.

Keep in mind that when updating PCB from the schematic, both the component and the connectivity changes are automatically transferred to

the PCB. If you update from the PCB to the schematic, however, only the component attribute changes are automatically transferred to the schematic. New components and connectivity differences are simply listed in the synchronization report.

Unit 8 Working with simulations

With Protel 99 SE you can perform an array of mixed-signal simulations on your design. The simulation engine works directly from your schematic, including multi-sheet designs, providing an easy way to investigate the performance of a circuit throughout the design cycle.

Protel's analog/mixed-signal simulation engine uses an enhanced version of Berkeley SPICE3f5/Xspice, allowing you to accurately simulate any combination of analog and digital devices without manually inserting D/A or A/D converters. This mixed-signal or mixed-mode simulation is possible because of the inclusion of accurate, event-driven behavioral models for digital devices, including TTL and CMOS.

Due to the complexity of digital devices it is generally not practical to simulate them using standard, non-event-driven, SPICE instructions. For this reason, Protel includes a special descriptive language that allows digital devices to be simulated using an extended version of the event-driven XSPICE. The digital devices included in the simulation-ready schematic libraries are modeled using the Digital SimCode language, a proprietary language created specifically for use with Protel.

The simulator allows unlimited circuit-level analog simulation and unlimited gate-level digital simulation. Circuit size is only limited by the amount of RAM you have in your system.

The types of analyses supported include: AC small signal, Transient, Noise and DC transfer, Monte Carlo analysis, parameter and temperature sweeping, and Fourier analysis.

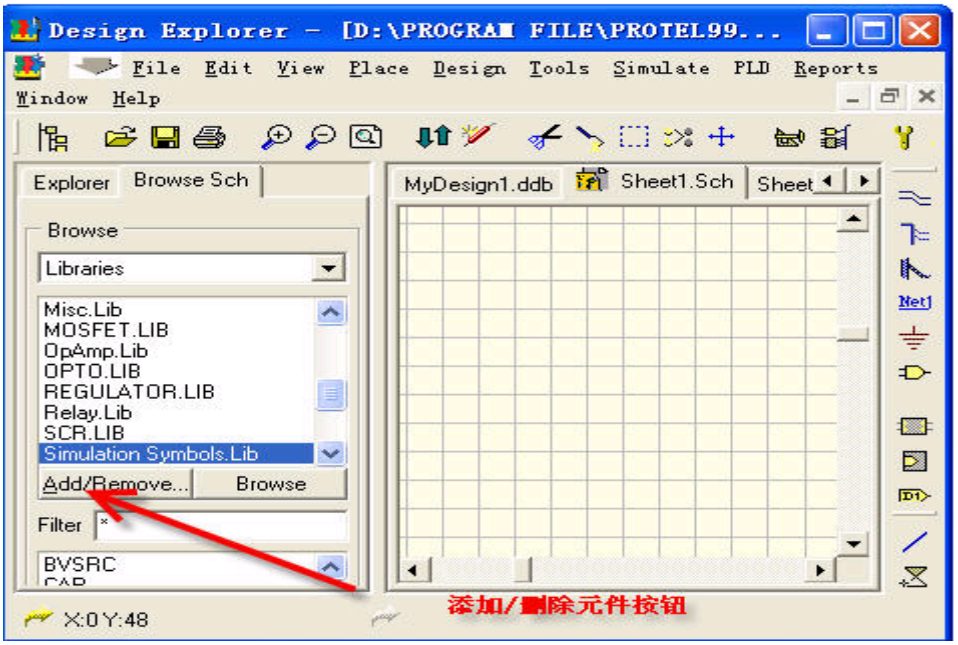
Before you can successfully simulate your circuit you need to ensure that your schematic documents contain all the necessary information. In general, the following rules must be adhered to before you will be able to run any of the available simulations:

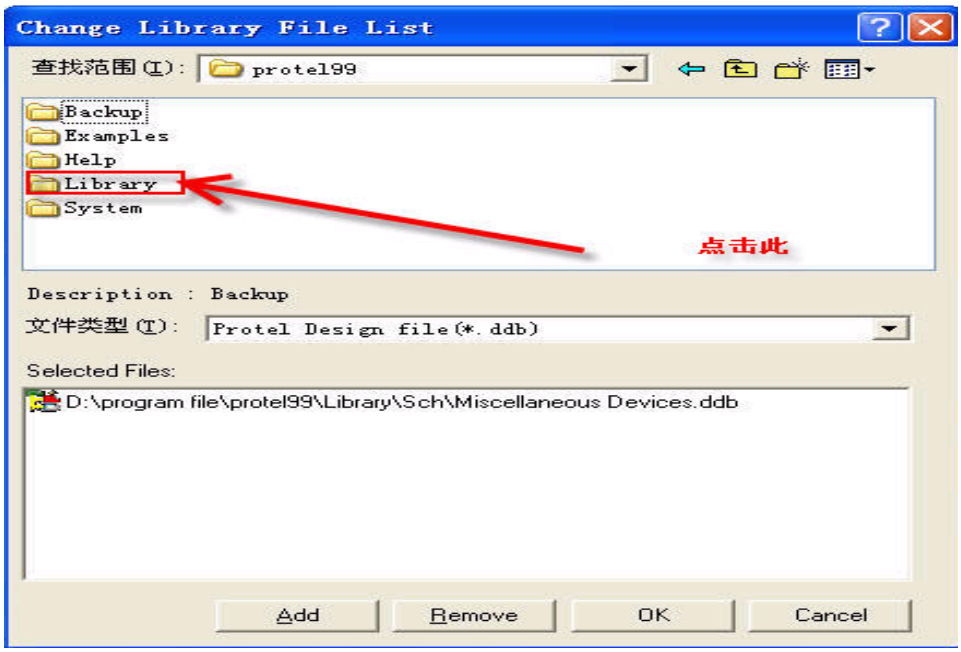
- All components and parts in the schematic must properly reference a simulation device model.
- You must place and wire up suitable signal sources to provide drive to the circuit during simulations.
- You must add net labels to identify nodes in the circuit for which you wish to plot simulation data.
- If necessary, you must set the initial simulation conditions of the circuit.

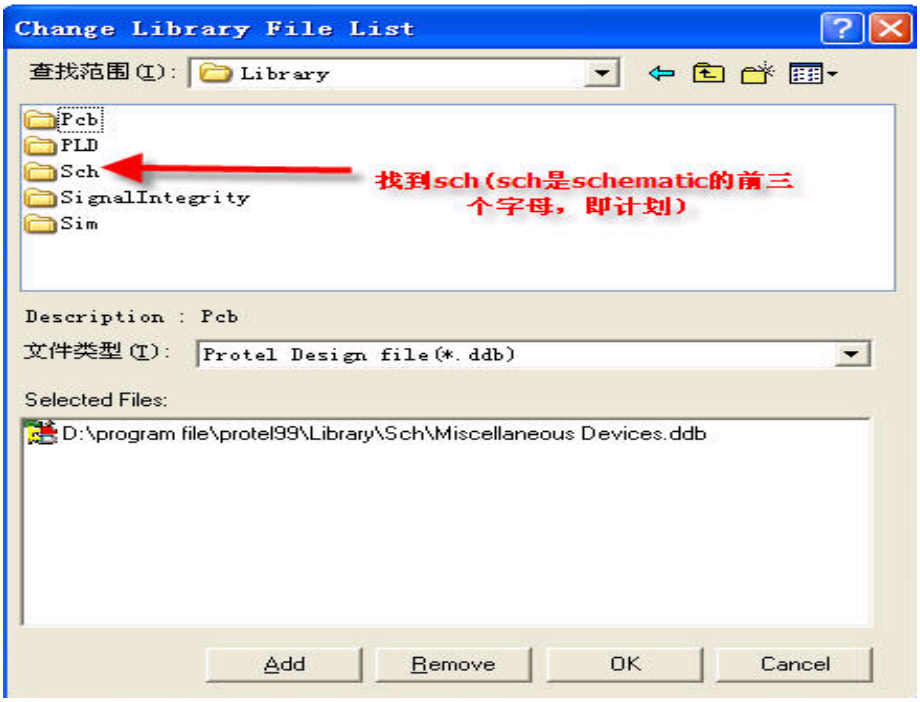
Part 1　Selecting simulation-ready schematic components

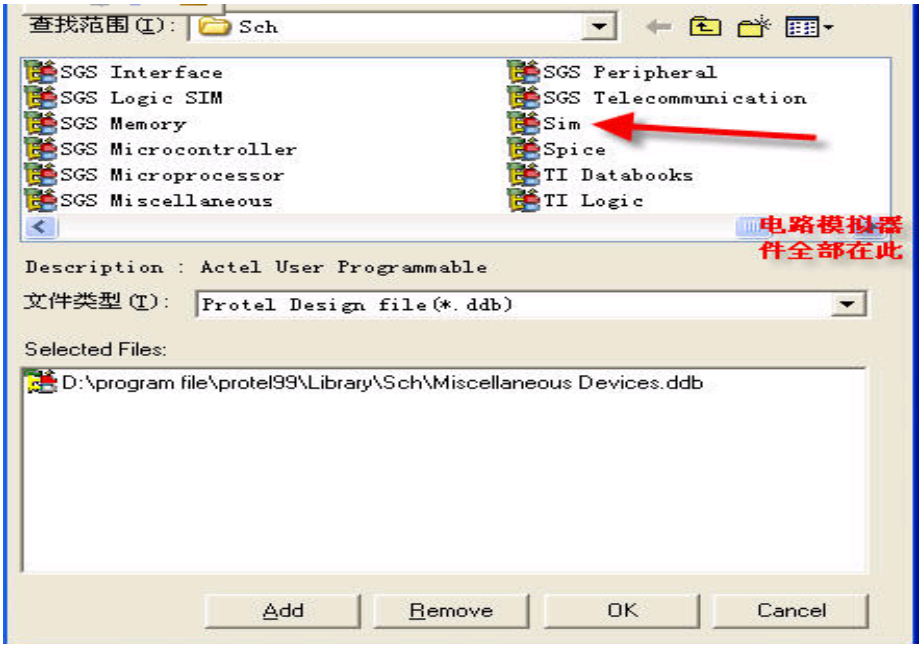
To perform simulation analyses, all parts placed on your schematic must contain special simulation-specific information which tells the simulator how these components are to be treated. In general this means that schematic parts must include a reference to an appropriate SPICE device model.

The simulation-ready schematic libraries can be found in the \Design Explorer 99 SE\Library\Sch\Sim.ddb within the drive and directory where you installed your Protel software.




Change Library File List
查找范围(I): protel99
Backup
Examples
Help
Library
System
点击此
Description : Backup
文件类型(T): Protel Design file(*.ddb)
Selected Files:
D:\program file\protel99\Library\Sch\Miscellaneous Devices.ddb
Add
Remove
OK
Cancel


Change Library File List
查找范围(I): Library
Pcb
PLD
Sch
SignalIntegrity
Sim
找到sch(sch是schematic的前三个字母，即计划)
Description : Pcb
文件类型(T): Protel Design file(*.ddb)
Selected Files:
D:\program file\protel99\Library\Sch\Miscellaneous Devices.ddb
Add
Remove
OK
Cancel



Simulation-ready Resistors

The Simulation Symbols.Lib library contains the following simulation-ready resistor symbols for use in schematics:

- RES (fixed resistor)
- RESSEMI (semiconductor resistor)
- RPOT (potentiometer)
- RVAR (variable resistor)

These symbols represent generic resistor types.

Simulation-ready Capacitors

The Simulation Symbols.Lib library contains the following simulation-ready capacitor symbols for use in schematics:

- CAP (fixed, non-polarized capacitor)

- CAP2 (fixed, polarized capacitor)
- CAPSEMI (semiconductor capacitor)

These symbols represent generic capacitor types.

Library Contains symbols for...

7segdisp.lib--generic seven-segment LED displays of different colors.

Buffer.lib--analog buffer ICs arranged by industry-standard part numbers.

CAmp.lib--current amplifier ICs arranged by industry-standard part numbers

Comparator.lib--comparator ICs arranged by industry-standard part numbers.

IGBT.lib--Insulated Gate Bipolar Transistors arranged by industry-standard part numbers.

Math.lib--various 2-port devices with mathematical transfer functions.

Misc.lib--Miscellaneous ICs and other devices.

Opamp.lib--opamp ICs arranged by industry-standard part numbers.

Opto.lib--generic opto-isolators.

Regulator.lib--IC regulators arranged by industry-standard part numbers.

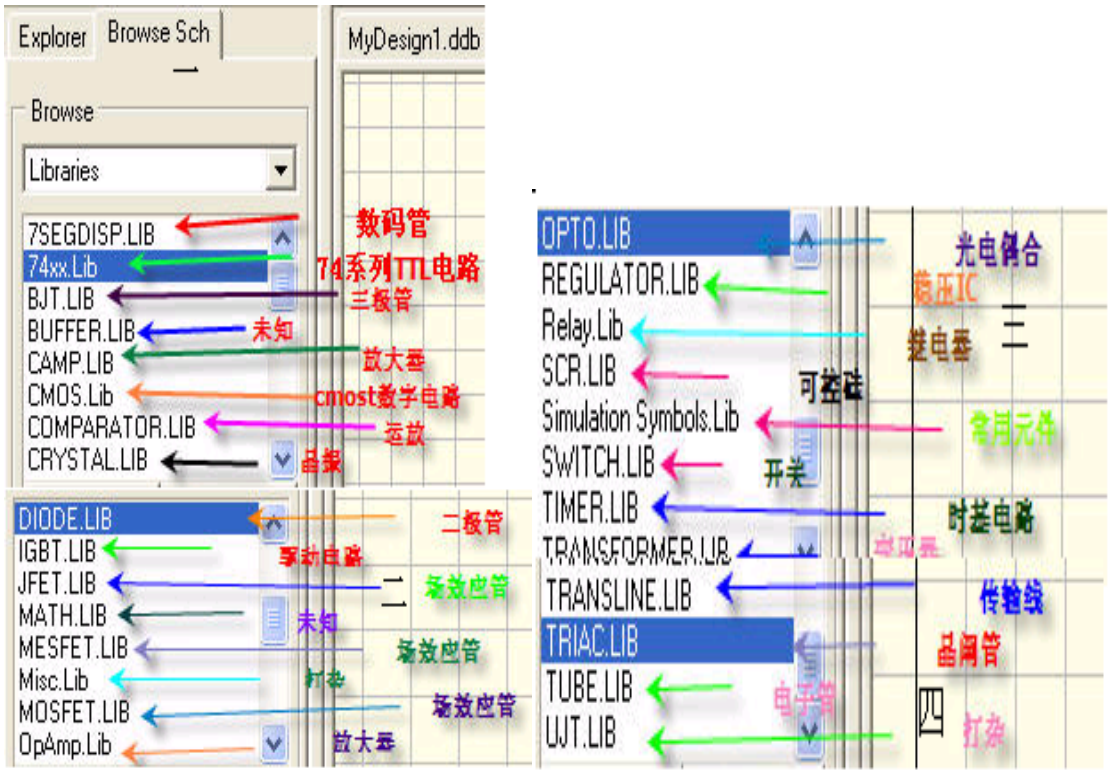
SCR.lib--Silicon Controlled Rectifiers arranged by industry-standard part numbers.

Timer.lib--555 timer ICs.

Triac.lib--Triacs arranged by industry-standard part numbers.

Tube.lib--various valve or tube devices.

UJT.lib--various Unijunction Transistors.



Part 2 Creating digital simulation components

Due to the complexity of digital devices it is generally not practical to simulate them using standard, non-event-driven, SPICE instructions. For this reason, Protel's simulation engine includes a special descriptive language called Digital SimCode that allows digital devices to be simulated using an extended version of the event-driven XSPICE. The

digital devices included in the Protel simulation-ready schematic libraries all reference Digital SimCode models.

Digital SimCode is a proprietary language created specifically for use with Protel, and devices created with it are not compatible with other simulators, nor are digital components created for other simulators compatible with Protel.

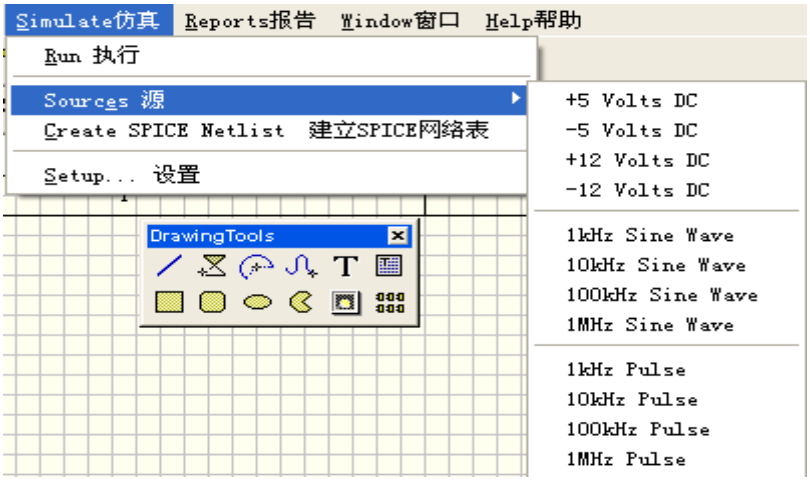
Creating a simulation-ready digital component is similar to creating any simulation-ready component, and you should familiarize yourself with the Creating your own simulation-ready components topic (see the Links section below) before attempting to create digital simulation components.

The main difference between digital components for simulation is that:

- digital devices include hidden power and ground power pins in each schematic symbol (VCC or VDD, and GND), and these pins are automatically connected during netlisting. The simulator uses these net names by default, so for a digital-only design it is not necessary to include sources to power these components. By default, VCC = 5V and VDD = 15V.
- digital devices reference an intermediate model (.MDL file) that simply calls the Digital SimCode device description.

Part 3　Adding simulation sources to a schematic

Once you place a source from the library, double-click on the source symbol to edit its properties. See the topics dealing with specific source types for information on setting the parameters for each source type.



Part 4　Identifying simulation circuit nodes

Before a simulation is performed on a circuit, a SPICE netlist is produced from the schematic. To enable the circuit to be netlisted, each node in the circuit is given a unique default name. These node names are then used to identify nodes during simulation data collection.

In order to easily identify points of interest in you circuit, you must identify these points using Net Labels on the schematic. A Net Label allows you to assign names such as VIN, VOUT, CLOCK, etc. to nodes

of a circuit, thereby making it possible to easily identify the signals at these nodes during a simulation.

Before running a simulation, place Net Labels at all points in the schematic for which you want to plot simulation data. The Net Label name will then be used in the netlist to identify these nodes. You will then be able to choose these points to plot from the **Analyses Setup dialog** (Simulate→Setup)

Part 5 Running simulation analyses

To run a simulation, with the schematic document active select **Simulate→Run** from the menus. This initiates a simulation run using the current configuration of the **Analyses Setup dialog**.

To configure the analyses before running the simulation, with the schematic document active select **Simulate→Setup** from the menus to open the **Anlyses Setup dialog**. You can run the simulation directly from the Analyses Setup dialog by pressing the Run Analyses button within the dialog.

As the simulation runs, a simulation waveform tab will open automatically to display the results of the analyses.

If an error is encountered during a simulation run, you will be asked if you want to view the errors. If you answer yes, an error file will be

created and displayed.

To view the SPICE netlist derived from the schematic, with the schematic document active select **Simulate →Create SPICE Netlist** from the menus to generate and display the netlist for the circuit. This is often useful for tracking down circuit drafting errors that cause simulation errors.

实训一

一、 实验/实训内容

1、 阅读国家标准 GB/T 4728 相关内容，规范绘制电路图。

2、 声光控楼梯灯电路如下图所示，在 protel 99 Se 中画出试它的原理图，元件清单如下表所示.。

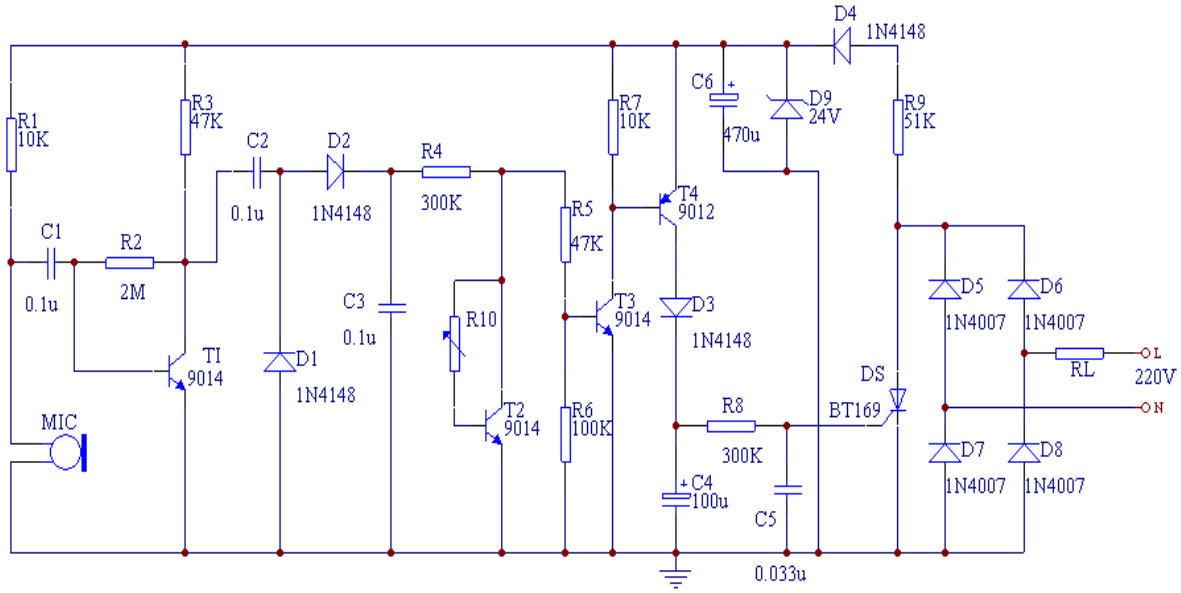


图 1-1

Used	Part Type	Designator	Footprint
3	0.1u	C1 C2 C3	RAD0.1
1	0.033u	C5	RAD0.1
4	1N4007	D5 D6 D7 D8	DIODE0.4
4	1N4148	D1 D2 D3 D4	DIODE0.4
1	2M	R2	AXIAL0.4
2	10K	R1 R7	AXIAL0.4
1	24V	D9	DIODE0.4
2	47K	R3 R5	AXIAL0.4
1	51K	R9	AXIAL0.4
1	100K	R6	AXIAL0.4
1	100u	C4	RB.2/.4
2	300K	R4 R8	AXIAL0.4
1	470u	C6	RB.2/.4
1	9012	T4	TO-92A
3	9014	T2 T3 T1	TO-92B
1	BT169	DS	TO-92A

二、 实验/实训要求

1、 设置图纸大小为 A4，水平放置，其它采用默认设置，填写标题栏中相关内容。

2、 工作光标为小 900、自动滚屏功能打开、取消自动放置节点，可取消 30 次操作。

3、 指定文档默认模板为 C:\99 SE 例子中的任一个，把该原理图更名为 1.sch 保存 d:上自己的目录中。

三、 实施指导

1、新建数据库文件

第一步：利用计算机基础操作知识，我们在计算机的硬盘 D 上建立自己的文件夹，以自己的班号姓名为目录名，如：电信 05308 王芳。

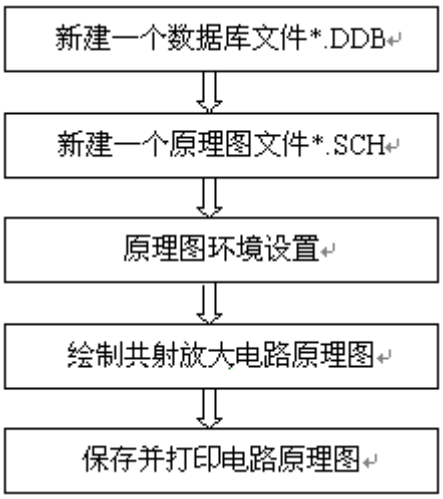


图 1-2　绘制电路原理图的过程

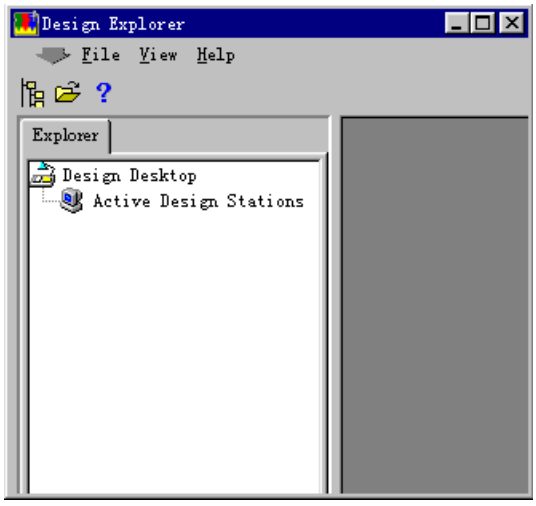


图 1-3

第二步：启动 Protel 99 SE 软件，利用 File/New 菜单命令打开新建项目对话框。

第三步：在图 1-4 新设计数据库（New Design Database）对话框中，设计存贮类型（Design Storage Type）选为 MS Access Database；数据库文件名（Database File Name）*.ddb；再通过浏览按钮 Browse... 来修改新数据库存放目录（Database Location）为 D:\电信 05308 王芳。

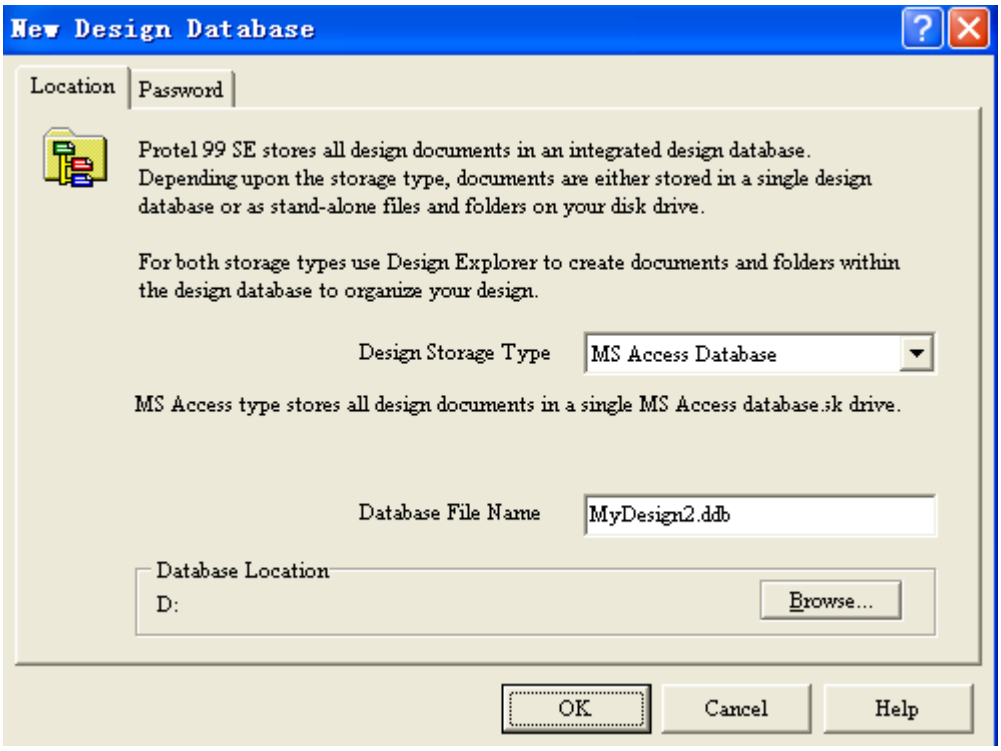


图 1-4

第四步：点击 OK 按钮后，一个新数据库文件 DDB 就建立好了。

2、新建原理图文件

第一步：如图 1-5 所示，进入 Protel 99 SE 基本设计环境界面里，执行 File/New 命令（或双击 Documents 图标，在进一步打开的 Documents 空白处点击鼠标右键，选择快捷菜单中 “NEW”命令），调出新文件 “New Documents”对话框。

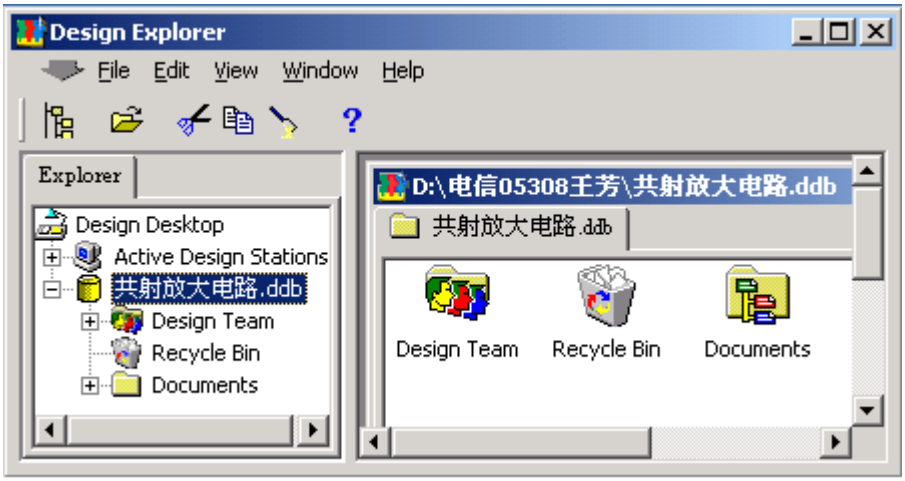


图 1-5　基本设计环境界面

第二步：在“New Documents”文件设计对话框中，选择原理图文件设计图标，如图 1-6 所示。

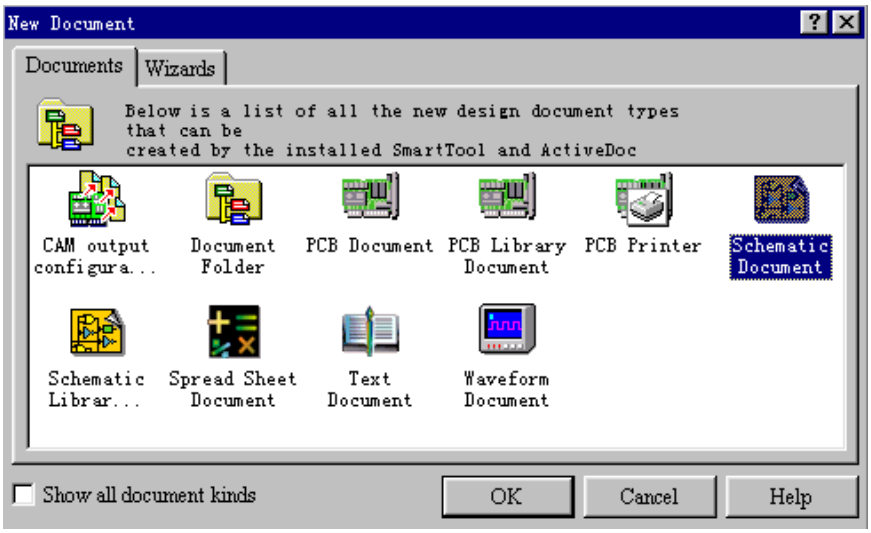


图 1-6　文件设计管理器

第三步：双击原理图文件设计图标（或选中原理图文件设计图标后单击 OK 按钮），输入原理图设计文件名称，就建立了一个未打开的空白原理图设计文档，如图 1-7 所示（注意：所有原理图文件扩展名都应为.sch）。

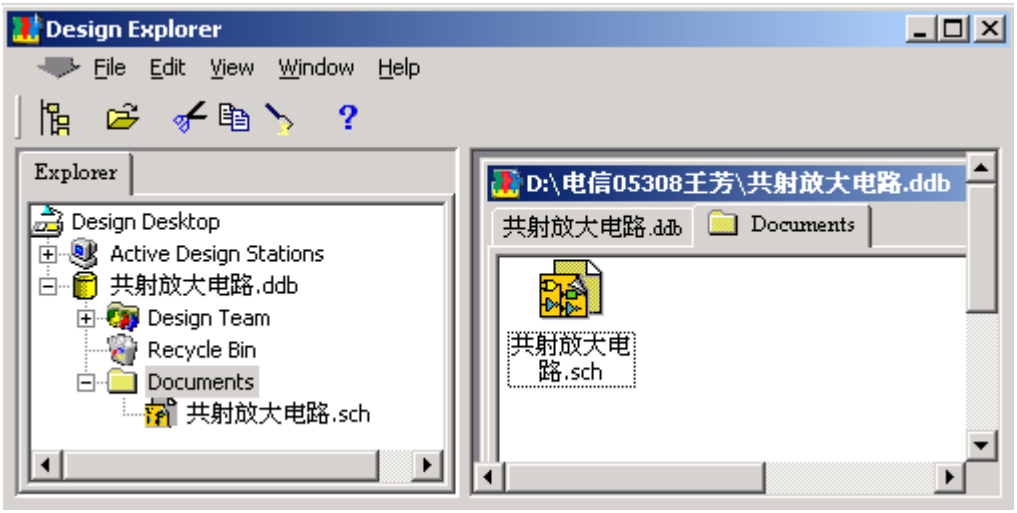


图 1-7

3、添加、卸载元件库

第一步：用鼠标单击设计管理器的 Browse Sch 选项卡，再单击 Add/Remove 按钮或执行菜单命令 Design/“Add/Remove Library”，系统将弹出“增加/删除元件库”对话框如图 1-8 所示。

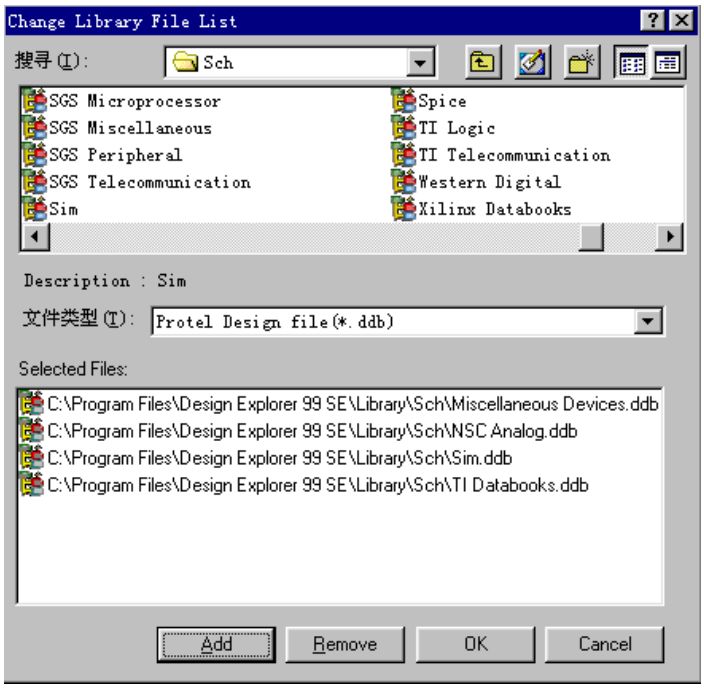


图 1-8　“元件库添加/删除”对话框

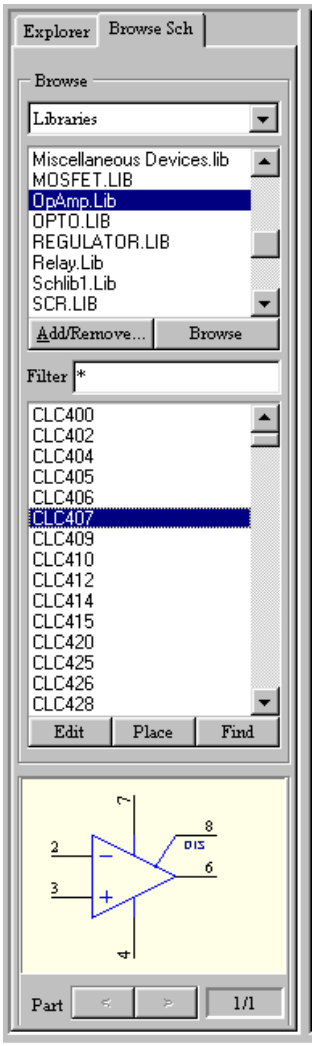


图 1-9 元件库管理器

第二步：在路径 C：\Program Files\Design Exploer 99 SE\Library 中找到 Sch 目录，双击该目录名，在打开的 Sch 目录里找到所需要元件库文件，然后双击该库文件名或点击 Add 按钮，此元件库文件就会出现在 Selected Files 下拉框中，如图 1-8 下半部分所示。元件库文件扩展名为.ddb，它是一个大型数据库文件，里面包括多个小型元件库 (*.lib 文件)，这是 Protel 99 SE 的一大特点。

技巧：一般电阻、电容等常用元件放在 miscellaneous Device.ddb 库中，常用的 TTL、CMOS 数字集成电路、运算放大器、集成稳压电源等放在 Protel Dos Schematic Libraries 元件库中。

第三步：选中所需元件库后点击 OK 按钮，完成元件库添加工作。利用设计管理器的 Filter（过滤）条件“*”，可将该元件库中每个元件详细内容（名称、元件原理图符号、元件上功能模块数）显示在设计管理器的下半部分，如图 1-9 所示。

第四步：当要卸载某一个元件库时，则需重新执行步骤一、步骤二操作，如要卸载 NSC analog.ddb 元器件库，可在图 1-7 所示对话框中的 Selected Files 框内选取要卸载的 NSC analog.ddb 元件库名，点击 Remove 按钮可卸载掉 NSC analog.ddb 库。

4、绘制共射放大电路原理图

第一步：放置元器件。

▲ **技巧 1**：在放置元件过程中按 Space 键可以旋转元件，改变元件放置方向。

▲ **技巧 2**：在放置元件时按 X 键实现水平镜像，按 Y 键实现垂直镜像，

▲ **技巧 3**：启动菜单 View 下的 Snap On（定位栅格）和 Visible（可视栅格）两个参数，使我们在放置元件、连接电线时才整齐美观，操作方便。

第二步： 编辑各元器件属性。

▲ **技巧 1**：也可在放置元件时按 Tab 键则系统会自动打开该元件的属性对话框，实现对其属性内容的修改。

▲ **技巧 2**：通过修改元件属性对话框 Graphical Attrs 页的 Orientation 栏角度同样可以改变元件放置的位置，如图 1-10 所示。

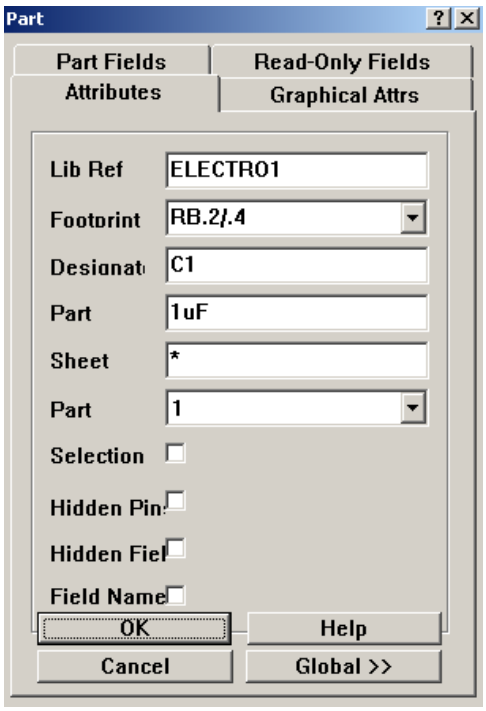


图 1-10 C1 属性对话框填写

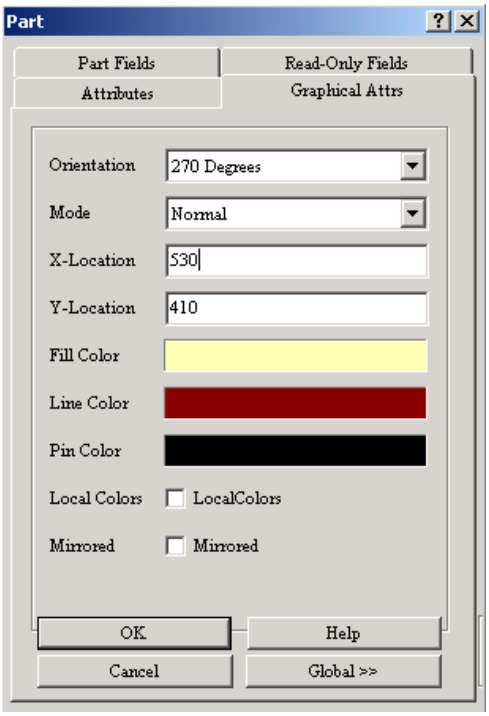


图 1-11 修改元件放置角度的对话框

第三步：放置电连接线。放置电连接线目的是按照电路设计要求实现网络的实际连通。放置电连接线时，可单击 Wiring Tools 工具栏上  按钮或执行菜单命令 Place/Wire。

第四步： 放置电连接点。放置电连接线时系统会给出一些节点，单击 Wiring Tools 工具栏上  按钮或执行菜单命令 Place/Junction 后，移动鼠标到线段交叉位置上单击鼠标左键就可在此处放置一个节点。

第五步： 放置电源 VCC、GND。电源/地线也是电路图中不可缺少的电气对象，使用菜单命令 Place\Power Port 来放置电源/地线时，按 Tab 键，系统弹出 Power Port 属性对话框，在 Net 栏填写 VCC 或 GND 网络名称、在 Style 栏选取所需的电源/地线的形状，如图 1-12。

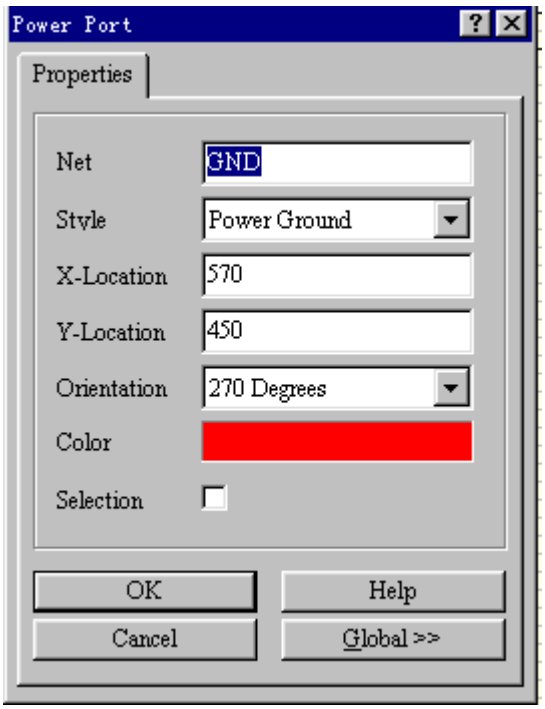


图 1-12　电源属性对话框

▲　**技巧 1：**当需要总体观察所绘电路时，用鼠标对准电路中心或所关心的元件，按 Page Up 键放大图纸或按键 Page Down 缩小图纸。

5、保存并打印共射放大电路原理图

第一步：　保存原理图文件：执行菜单命令 File/Save 或点击常用工具栏上的图标就可直接保存电路图到一开始建立数据库*.DDB 时指定的 D：\电信 05308 王芳目录中。

第二步：打印输出电路原理图：

实训二

一、 实验/实训内容

3、 创建自己的 my.lib 元件库，按下图修改相关元件外形并保存 my.lib 中。

4、 在 protel 99 Se 中画出试它的原理图，元件清单如下表所示。

5、 对下图进行 ERC 电气规则检测，并根据其报告中的所指错误或警告修改电路图中相关内容。

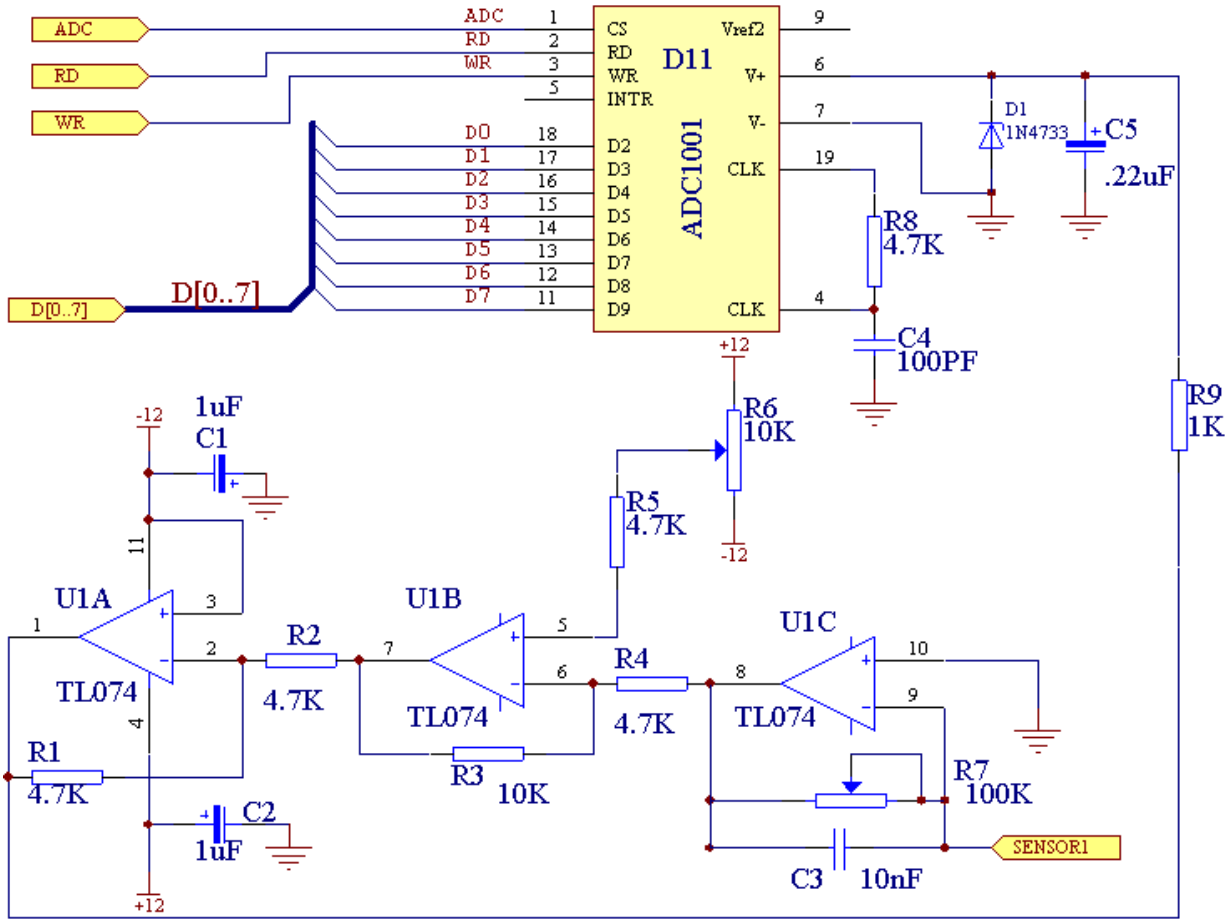


图 2-1

Used	Part Type	Designator	Footprint
1	.22uF	C5	RB.2/.4
1	1K	R9	AXIAL0.4
1	1N4733	D1	DIODE0.4
2	1uF	C1 C2	RB.2/.4
5	4.7K	R1 R2 R4 R5 R8	AXIAL0.4
1	10K	R3	AXIAL0.4
1	10K	R6	VR1
1	10nF	C3	RAD0.1
1	100K	R7	VR1
1	100PF	C4	RAD0.1
1	ADC1001	D11	DIP20
1	TL074	U1	DIP14

二、 实验/实训要求

a) 设置图纸大小为 A4，水平放置，其它采用默认设置，填写标题栏中相关内容。

b) 工作光标为大 90^0、自动滚屏功能打开、自动放置节点。

c) 写实验/实训报告，必须包含画该电路图的体会。

三、 实施指导

a) 掌握创建元件库和元件方法。

第一步：元件库编辑器启动。在当前设计管理器环境下，执行菜单命令 File/New，系统将显示“New Document”对话框，选择原理图元件库编辑器图标，系统在当前设计管理器中创建一个新元件库文件，修改文档名称为 mySchlib1.lib，双击进入原理图元件库编辑工作界面，如图 2-2-所示

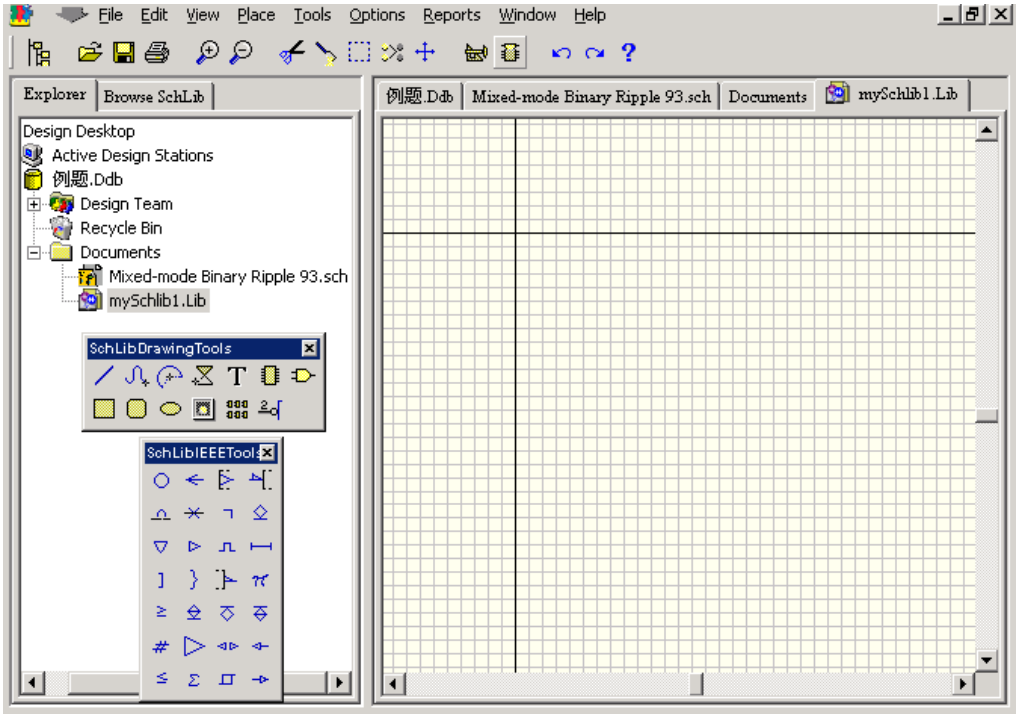


图 2-2　元件库编辑工作界面。

第二步：元件库编辑器环境设置。元件库编辑器的编辑区有一个十字坐标轴，将元件

编辑区划分为四个象限，即右上角为第一象限，左上角为第二象限，左下角为第三象限，右下角为第四象限。一般元器件编辑工作都在第四象限进行，将光标对准第四象限，用 Page Up 键将窗口放大到可以清楚地看到可视栅格。

第三步：绘制新的元件库

（1）绘制元件外框。

（2）放置引脚，注意在放置引脚时可按 Space 键确定引脚角度。

（3）修改各个引脚的属性。依次双击各个引脚（或选中引脚后按 Tab 键），调出其相应的引脚属性对话框修改各项值，

▲ **技巧 1**：当用户需要输入字符上带有一横的字符时，可以使用“字符\”来实现。

如在引脚名处输入“G\2A” 来实现$\overline{G}$2A、输入“Y\7\” 来实现$\overline{Y7}$等。

（4）给元件命名。执行菜单命令 Tools/Rename Component…，调出元件更名对话框

（5）填写元件相关描述。执行菜单命令 Tools/Description…，调出元件描述对话框如图

2、调用自建元件库绘制较复杂电路图

第一步：单击 Add/Remove 按钮或执行菜单命令 Design/“Add/Remove Library”，将编辑/创建元件任务的例题中自创的元件库 mySchlib1.Lib 打开，使用自建元件绘图。

第二步：点击导线工具  按钮、总线工具  按钮、总线分支线工具  按钮放置导线、总线、总线分支线，并使用  按钮放置上相应的网络标号

第三步：使用一般端口工具  按钮放置端口，使用  工具处放置一个电源 VCC。

第四步：使用放置文本工具  按钮放置文本“，放置文本时按 Tab 键调出文本属性对话框，在对话框的 Text 处填写文本的内容。

3、电路图创建各种报表

第一步：电路原理图的 ERC 报表。打开原理图，执行菜单命令 Tools/ERC 后系统将会出现 Setup 选项卡对话框，我们根据需要设置电气规则检查各选项，点击 OK 按钮后，程序自动进入文本编辑器并生成相应的规则检查报告。

第二步：原理图网络表。执行菜单命令 Design/Create Netlist，系统弹出创建网络表对话框，设置完对话框后，点击 OK 按钮，系统将用记事本自动打开网络表文件，网络表格式如下：

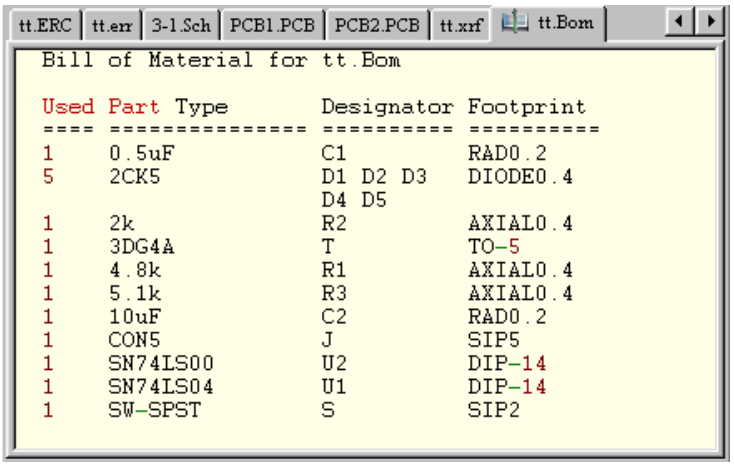
```
[                       ←开始描述一个元器件
C1                      ←元件编号
RAD0.2                  ←元件封装型号
0.5uF                   ←元件类型或标称值
                        ←三行空行


]                       ←结束一个元件的描述
```

(　　← 一个网络描述开始
GND　　← 网络名称（该网络名是用 Place/Net label 命令手动给定的）
D2-2　　← 网络连接的第一个分支，格式为“元件编号—元件引脚”
D4-1　　← 网络连接的第二个分支，格式为“元件编号—元件引脚”
J-4　　← 网络连接的第三个分支，格式为“元件编号—元件引脚”
R2-1　　← 网络连接的第四个分支，格式为“元件编号—元件引脚”
T-3　　← 网络连接的第五个分支，格式为“元件编号—元件引脚”
U1-7　　← 网络连接的第六个分支，格式为“元件编号—元件引脚”
U2-7　　← 网络连接的第七个分支，格式为“元件编号—元件引脚”
)　　← 一个网络描述结束

4、元件列表

在原理图环境中，执行菜单命令 Reports/Bill of Material，调出产生列表向导对话框，点击 Next 键，程序自动形成后缀为*.BOM 元件列表文本文件。如下所示，元件列表文件中 Used 列为所用某种元件个数，Part Type 列为该元件类型，Designator 列为元件编号，FootPrint 列为元件封装类型。



元件列表

实训三

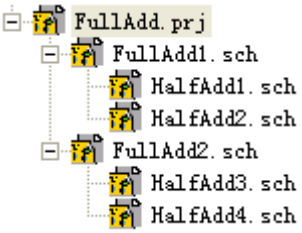
一、 实验/实训内容

1、 创建元件库 my.lib，在元件库中制作 DM74LS04、DM74LS08 和 DM74LS32 三个元件。

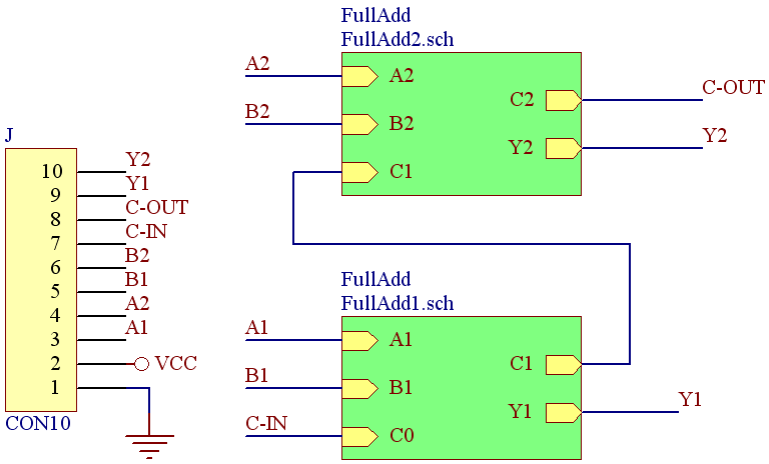
2、 在 Protel 99 Se 中画出下图所示的层次电路原理图，并给元件编号，元件清单如表格所示。

3、 对下图进行 ERC 电气规则检测，并根据其报告中的所指错误或警告修改电路图中相关内容。

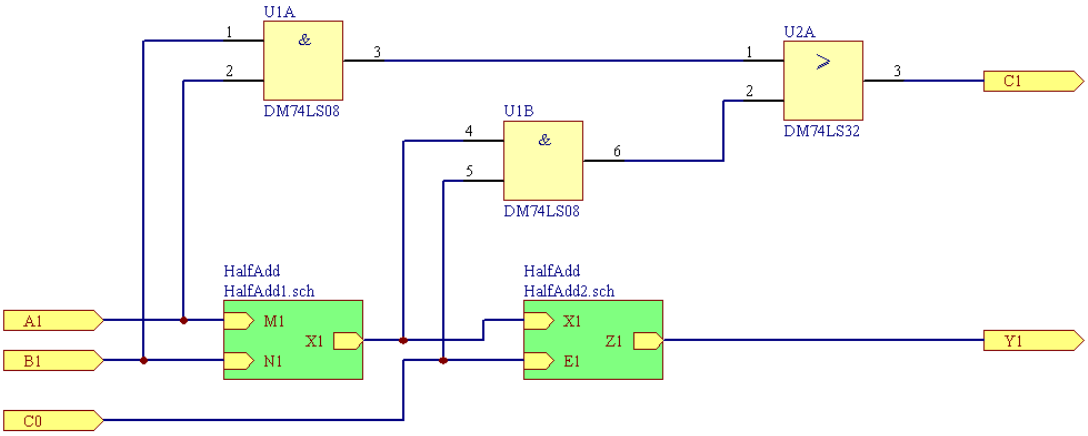
4、 创建该层次电路图的网络表及交叉参考表。



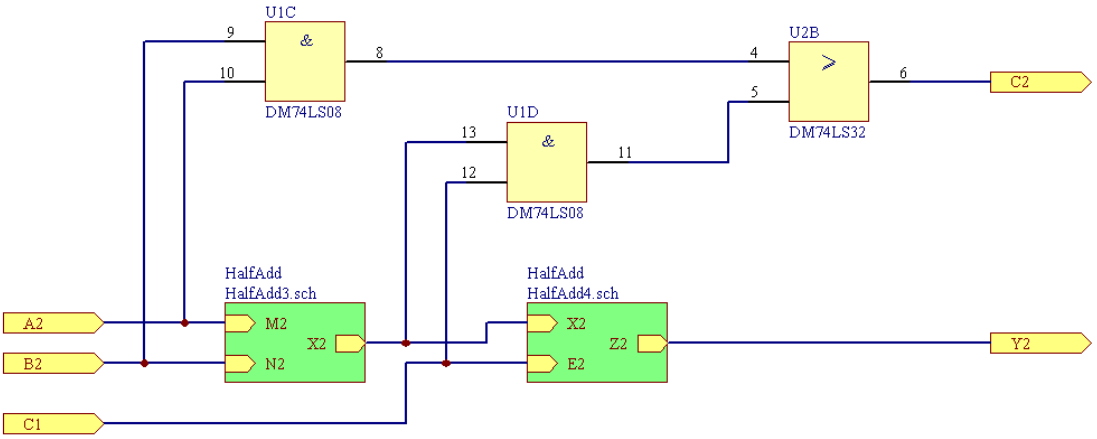
层次关系



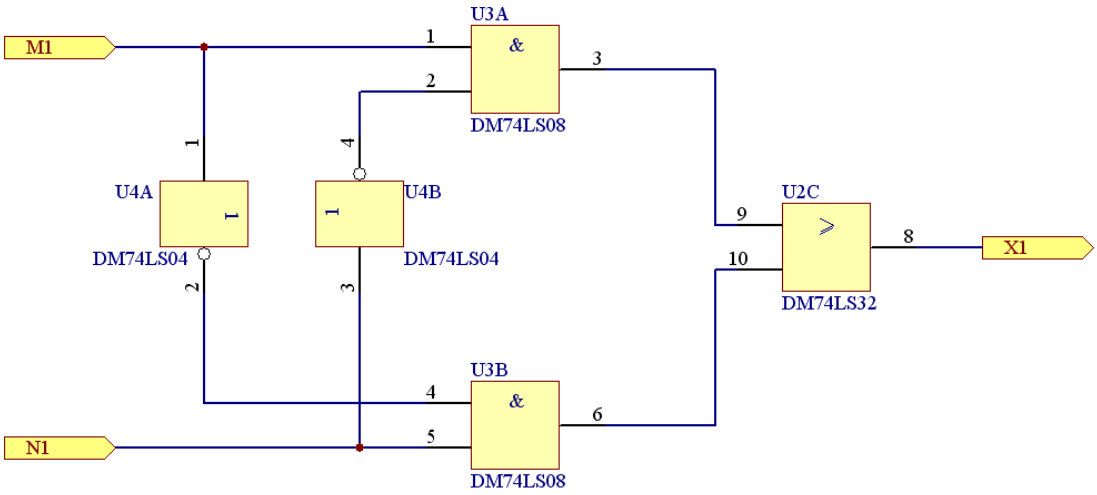
第一层图 FullAdd.prj



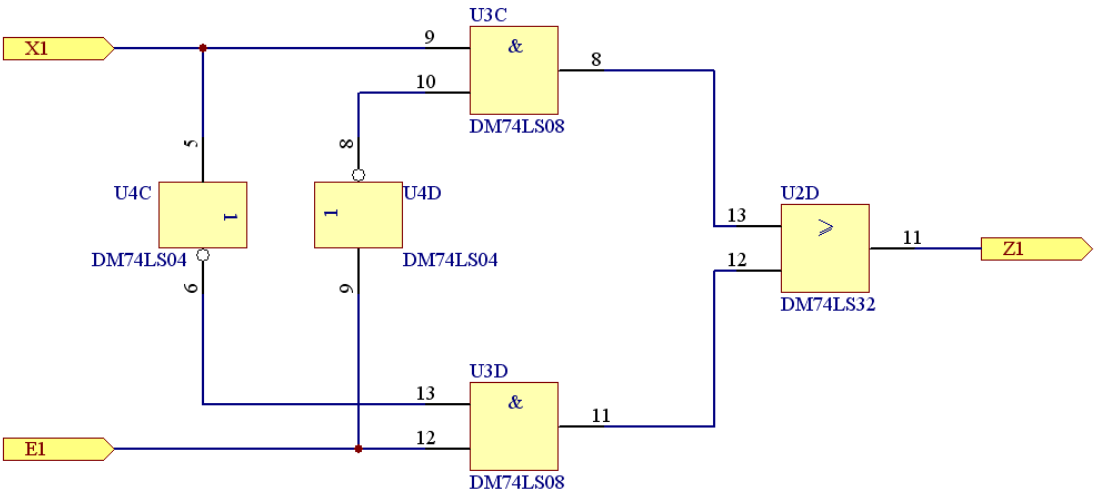
第二层图 FullAdd1.sch



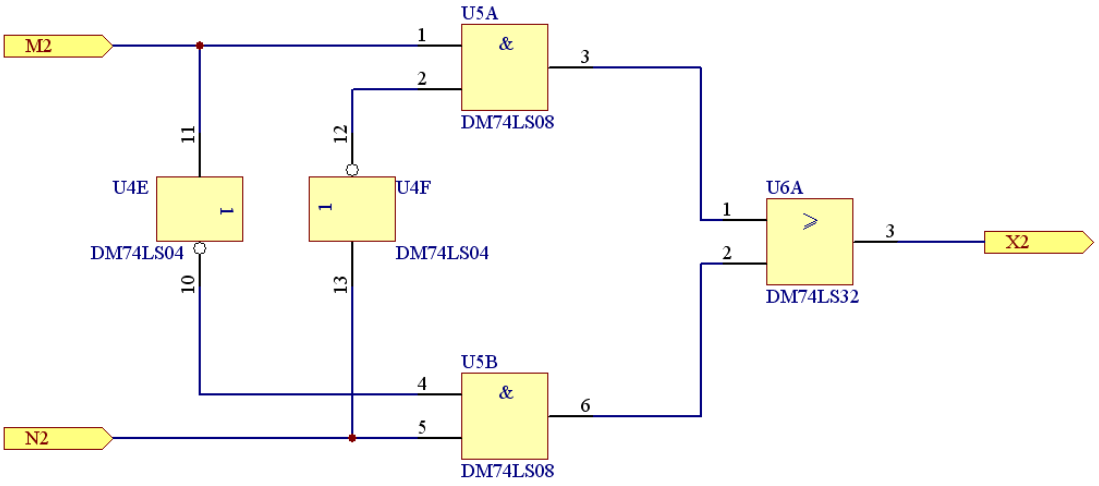
第二层图 FullAdd2.sch



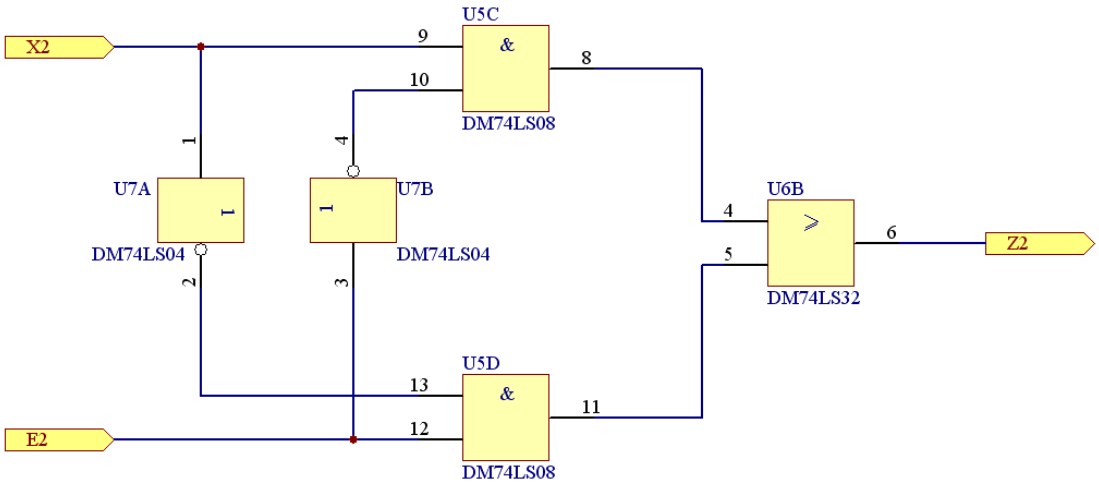
第三层图 HalfAdd1.sch



第三层图 HalfAdd2.sch



第三层图 HalfAdd3.sch



第三层图 HalfAdd4.sch

Used	Part Type	Designator	Footprint
1	CON10	J	SIP10
2	DM74LS04	U4 U7	DIP14
3	DM74LS08	U1 U3 U5	DIP14
2	DM74LS32	U2 U6	DIP14

元件清单

二、 实验/实训要求

1、设置图纸大小为 A4，水平放置，其它采用默认设置，填写标题栏中相关内容。

2、工作光标为小 90^0、自动滚屏功能打开、自动放置节点。

3、写实验/实训报告，必须包含画该电路图的体会。

三、 实施指导

1、创建元件库 my.lib，在元件库中制作 DM74LS04、DM74LS08 和 DM74LS32 三个元件。

2、绘制二位全加器电路图 FullAdd.prj（即第一层图）。

3、绘制第一位全加器电路图 FullAdd1.sch（即第二层图）。

4、绘制第二位全加器电路图 FullAdd2.sch（即第二层图）。

5、绘制第一个半加器电路图 HalfAdd1.sch（即第三层图）。

6、绘制另外三个半加器电路图 HalfAdd2.sch，HalfAdd3.sch，HalfAdd4.sch（即第三层图）。

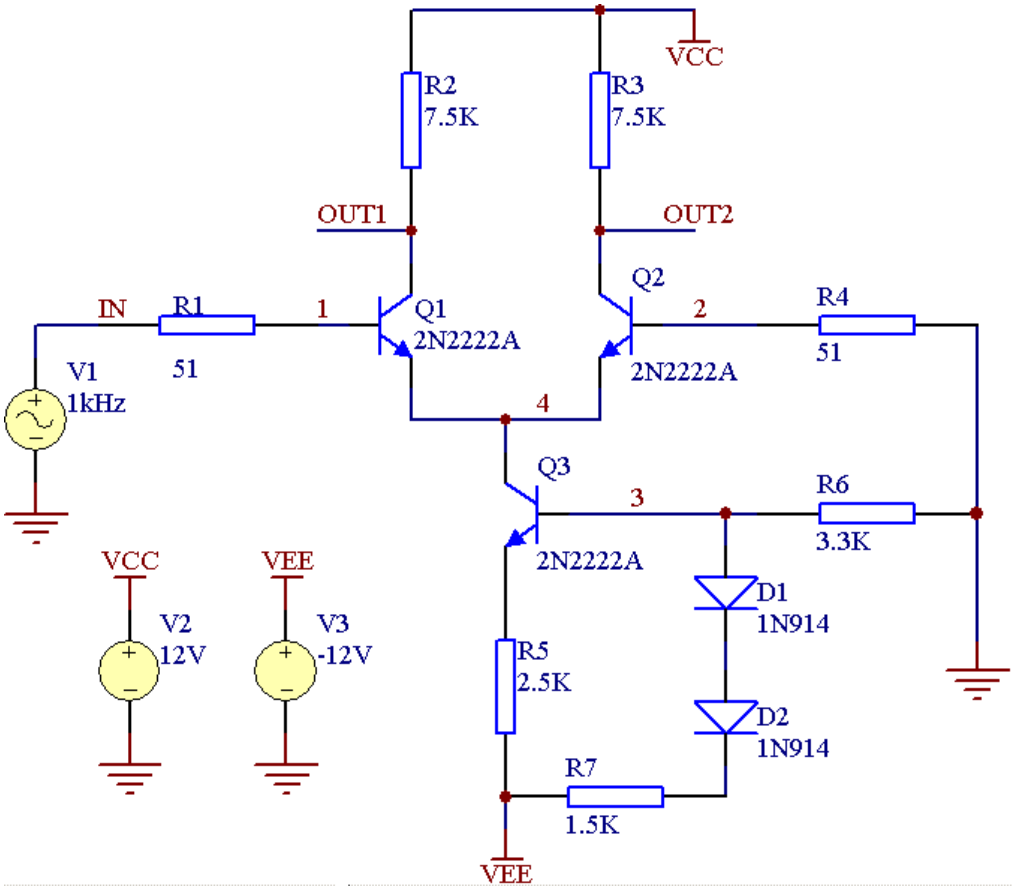
7、给层次电路图中的元件进行手动编号。

8、创建层次电路图的网络表。

9、创建层次电路图的交叉参考表

实训四

一、 实验/实训内容



4-1 仿真电路图

二、 实验/实训要求

a) 设置图纸大小为 A4，水平放置，其它采用默认设置，填写标题栏中相关内容。

b) 画出仿真后 IN、1、2、3 点的波形，总结仿真该电路的体会。

三、 实施指导

1、静态工作点分析

在此我们主要查看电路中相关节点电压和三极管的静态工作电流。电路具有合适的静态工作点是电路正常工作的必备条件。电路的静态工作点仿真分析步骤如下：

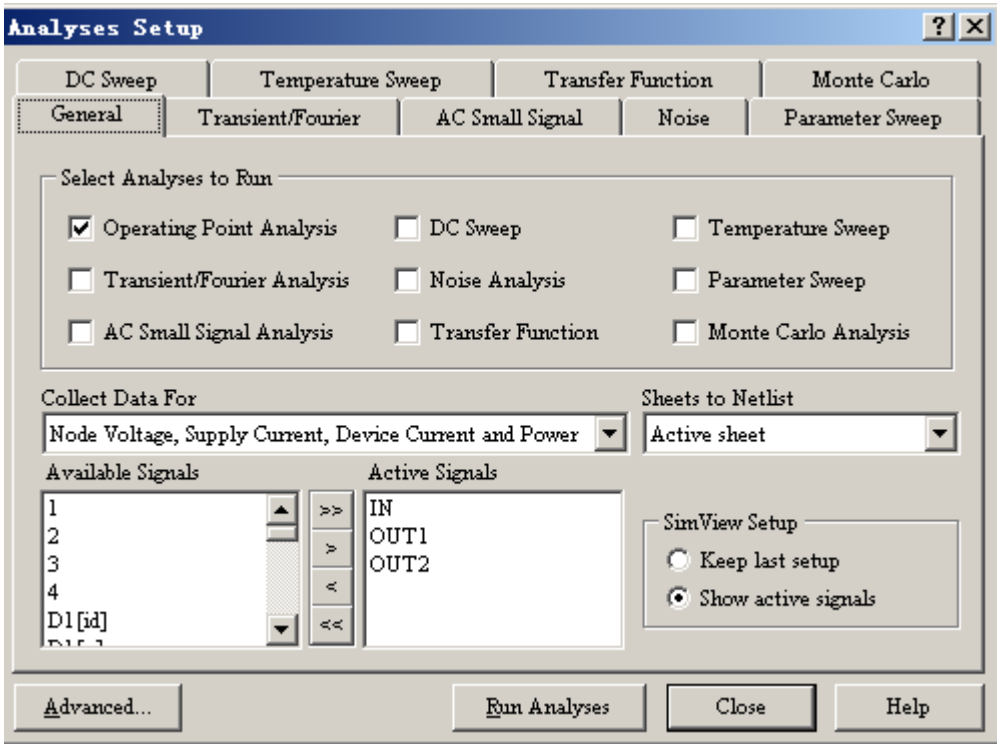
第一步：在原理图设计环境中，执行菜单命令“Simulate/Setup…”。

第二步：在图 4-2 所示对话框的 General 页中，只选择 Operating Point Analysis。

第三步：在 Active Signals 栏中选择 IN、OUT1、OUT2 三个信号。

第四步：选择 Show Active Signals。

第五步：单击 Run Analysis 按钮，可得到如图 4-3 所示结果。



4-2　对话框的 General 页设置

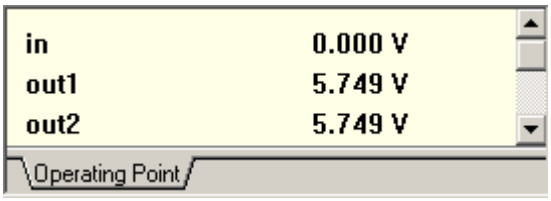


图 4-3　　静态工作点

2、瞬态/傅里叶分析

瞬态分析是一种非线性时域分析，它可以在给定激励信号的情况下，计算电路的时域响应。瞬态仿真分析步骤如下：

第一步：在原理图设计环境中，执行菜单命令“Simulate/Setup…”。

第二步：在图 4-2 所示对话框的 General 页中，选择 Operating Point Analysis、Transient/Fourier Analysis 两项。

第三步：在 Active Signals 栏中选择 IN、OUT1、OUT2 三个信号。

第四步：选择 Show Active Signals。

第五步： Transient/Fourier Analysis 如图 4-4 所示。

第六步：单击 Run Analysis 按钮，可得到如图 4-5 所示结果。

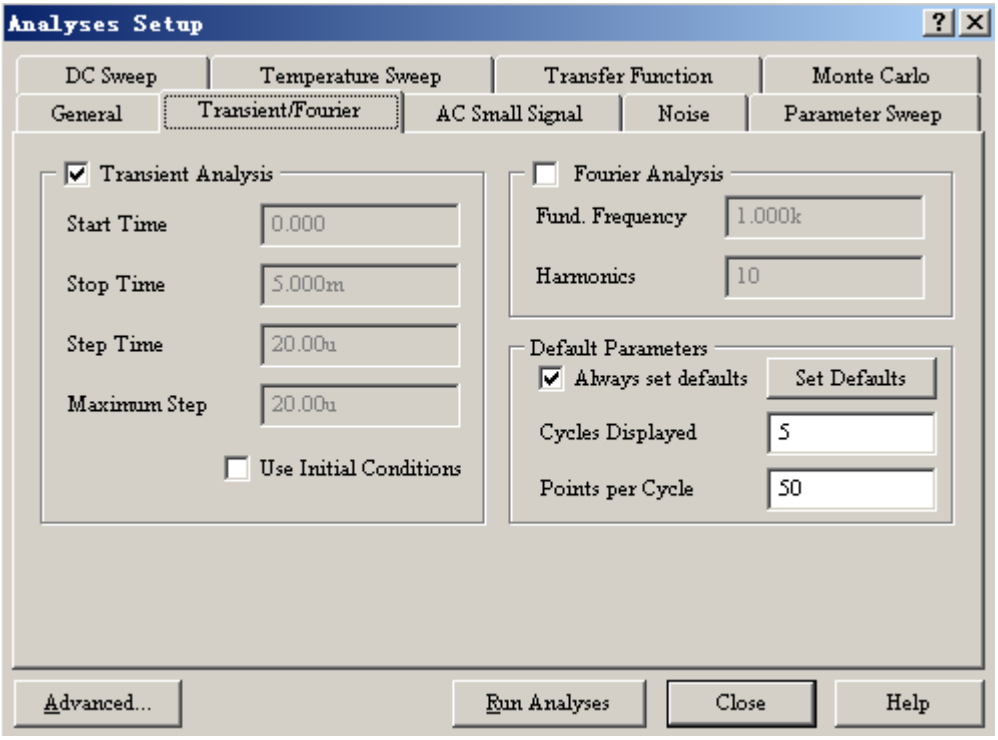


图 4-4 Transient/Fourier Analysis 页设置

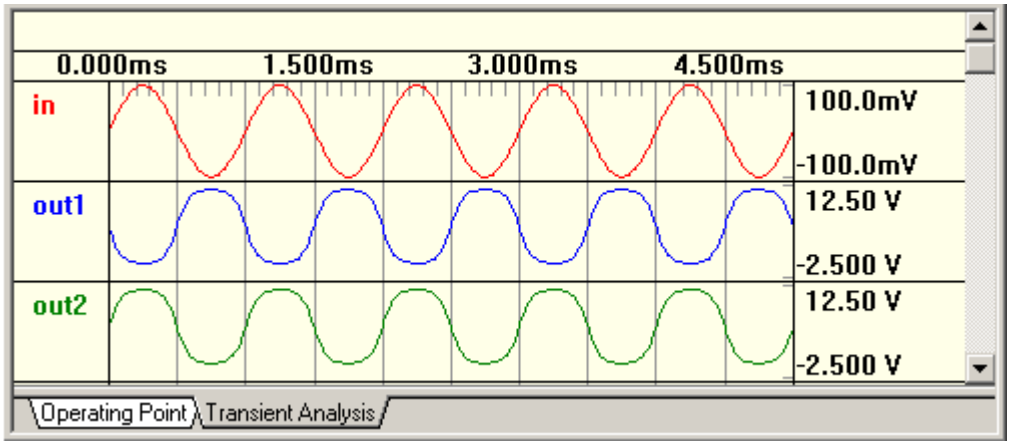


图 4-5　瞬态/傅里叶分析结果

可以适当调节电路的参数以达到改善输出波形质量，从波形图中可以知道 out1=-out2。

3、交流小流信号分析（频率响应）

交流小流信号分析时在 General 页应选择 Operating Point Analysis、AC Small Signal 两项，AC Small Signal 页的设置如图 4-6 所，仿真结果如图 4-7 所示。从仿真结果可以知道本电路的频带宽度约为 1MHZ。

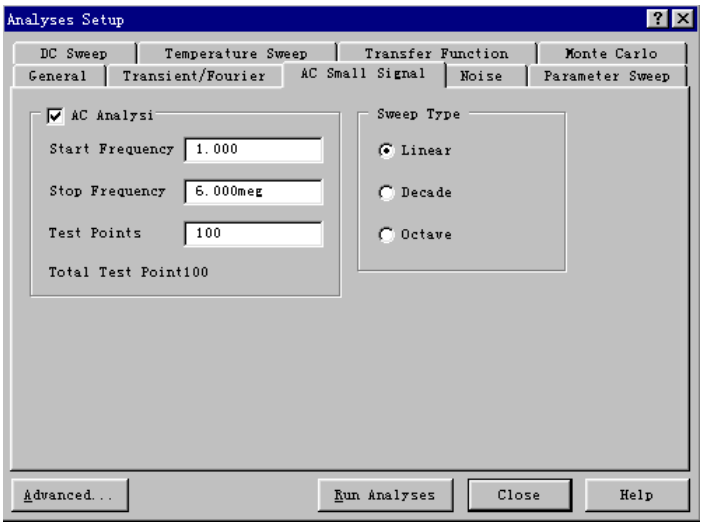


图 4-6　频率响应公析的参数设置

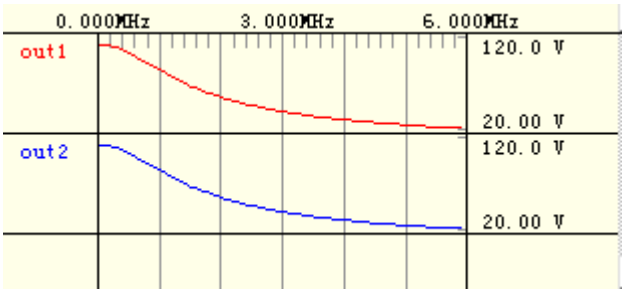


图 4-7　频率响应分析结果

4、温度扫描分析

差动放大电路有利抑制温度漂移，该电路在不同温度（-20^{0}C——110^{0}C）条件下工作，电路的性能不会有太大变化，Temperture Sweep温度扫描页的设置如图 4-8 所示，输出信号 out2 的温度扫描分析结果如图 4-9 所示。

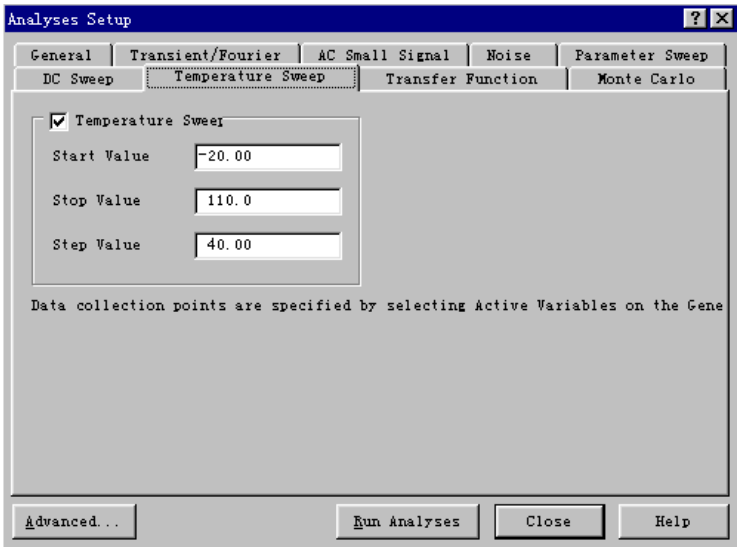


图 4-8　温度扫描分析设置

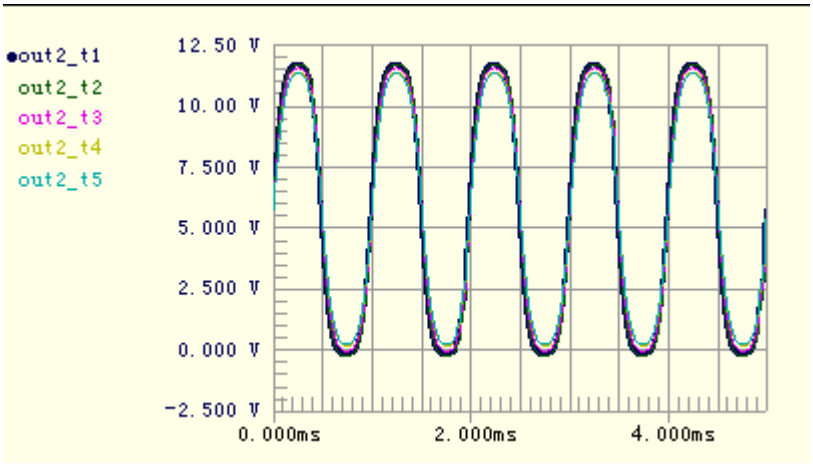


图 4-9　温度扫描分析结果

实训五

一、 实验/实训内容

在图 5-1 放大整形电路原理图基础上运用 Protel 99 SE 的 PCB 编辑器自动布局、布线方法设计出 PCB 图，如图 5-2，必须满足以下技术要求：

1、双面板，板框尺寸 3000mil×2000mil；

2、采用插针式元件；

3、镀铜过孔；

4、焊盘之间允许走一根铜膜导线，且最小间距 15mil；

5、最小铜膜导线宽度 35 mil，电源/地线的铜膜导线宽度为 60 mil，导线拐角 45º 。

6、对该 PCB 板进行设计规则检查及后续优化处理。

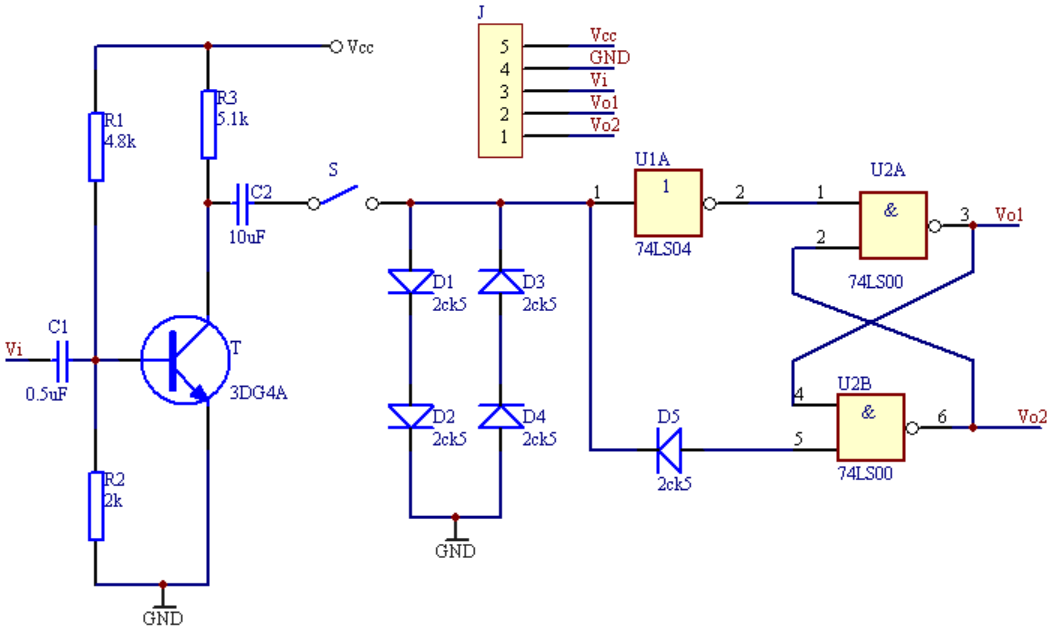


图 5-1

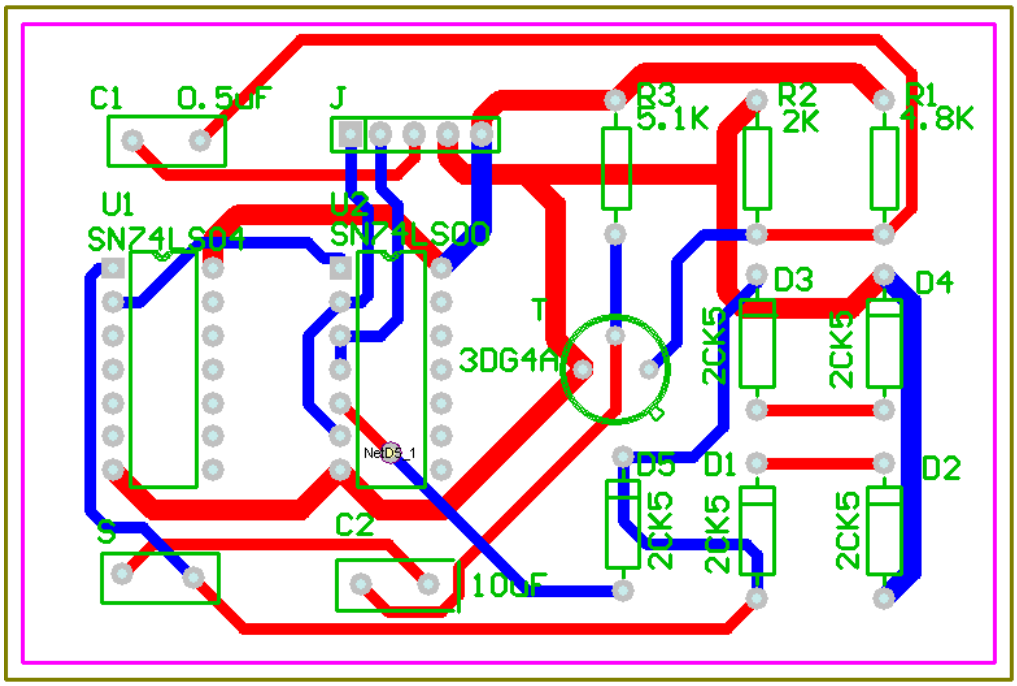


图 5-2

二、 实验/实训要求

1、按照实训内容中的技术要求完成双面印制电路板的自动设计。

2、根据设计规则检查结果分析 PCB 设计，并对不合理处加以修改。

3、总结本次实训/实验，并撰写实验/实训报告。

三、 实施指导

a) 规划电路板

（1）启动 PCB 向导：进入放大整形电路数据库(放大整形电路.ddb)的 Documents 界面后，执行菜单命令 File / New…或单击鼠标右键选择 New…，选择“Wizards”标签，双击“Printed Circuit Board Wizard”(印刷电路板向导)文件图标，进入 PCB 向导对话框。

（2）选择印刷板类型：单击 “Next”按钮后选择“Custom Made Board”——用户自定义印刷板尺寸。

（3 定义印刷板外型尺寸参数：单击 “Next”后选择印刷板外型为矩形（Rectangular），输入板宽度“Width”3000mil，高度“Height”2000mil（或单击 “Next”后输入外型尺寸）。其中物理边界（Mechanical Layer 4）与电气边界（Keep Out Layer）间距为 50mil，取消下端所有默认“ √ ”项。

（4）确定印刷板信号层结构：单击 “Next”进入，根据任务要求选择“具有金属化过孔”的双面板。

（5）选择过孔类型：单击 “Next”后选择“穿通形式过孔”，应尽量避免使用第二种“盲孔或掩埋孔”。

（6）选择多数元件封装方式：单击 “Next”后，根据任务要求选择“穿通式封装元

件”，并指定两元件引脚之间走线数目为 1。

（7）设置布线规则：单击 “Next”，根据任务要求设置导线最小宽度 35mil，过孔外径和孔径最小值为默认值，最小线间距 15mil。

（8）保存模板：单击 “Next”保存模板，单击“Finish”后即完成印刷板创建操作过程，显示出印刷板边框外形。

2、装入网络表和元件封装

（1）装入元件封装库：PCB 元件封装库存放在“Design Explorer99SE\Library\Pcb”文件夹内的三个不同的子目录下，常用元器件封装在 Generic Footprints\Advpcb.ddb 中，系统安装后默认装入其中的 PCB Footprint.lib。若使用了不在此库中的元件封装，则需要将所在封装库文件装入 PCB 设计环境中，否则将因系统不认而出错。

执行菜单命令 Design/Add/Remove Library…，或单击窗口左侧的“Browse PCB”标签，在下拉选项中选择“Libraries”，点击 Add/Remove….按钮，“添加/删除元件库”对话框，找到原理图中的所有元件所用的元件封装库，单击 Add 按钮，即可添加完成。

（2）调入网络表：将由原理图生成的网络表文件调入 PCB 设计环境中，要求电路原理图、网络表和 PCB 元件的名称、元件结构和封装形式等内容一一对应。 它首先将调入的网络表翻译成可以执行的网络宏(Netdist Macro)命令，再将元件封装和网络放置到电路板上。

1）执行菜单命令 Design / Load Nets…。

2）单击“Browse…”按钮，找到网络表文件“放大整形电路.NET”。

（3）改错：若窗口右侧的“Error”项中有错误报告，同时列表窗下提示错误总数为 10，常见宏命令错误：

Node not found：找不到元件某一焊盘。原因是元件在原理图中的电气图形引脚编号与元件在 PCB 图中封装图引脚编号不一致。

Component not found：找不到元件封装图。原因是原理图中给定的元件封装形式在封装库文件（.Lib）中找不到，有可能是元件封装名不正确，或者是特殊封装形式在封装图形库中不存在。

分析出错原因，发现全部是二极管问题，原因在于五个二极管在原理图中的电气引脚号分别为 1、2，但是所给定的二极管封装（DIODE0.4）在装入的 PCB Footprint.lib 封装库中的封装引脚号却为 A、K，两者不一致，需要统一编号。所以重新回到网络表“放大整形电路.NET”文件中，将所有二极管的“1”脚均改为“A”脚，“2”脚均改为“K”脚，如图 8-23 所示，修改完成后重新保存该网络表文件。依照上述操作重新调入修改后的网络表，直至无错误信息报告为止。

注意：另一种修改方法。亦可选定一条错误信息后，单击鼠标右键选择“Properties…”命令，在对话框中将 Node 中的“1”改为“A”，然后对该条修改过的信息单击鼠标右键，选择“Validate”命令，此时错误信息自动更新消失。

（4）执行：单击 Execute 按钮，即可调入网络表与元件。至此由原理图“放大整形电路.Sch”生成的网络表“放大整形电路.NET”已被正确调入当前的 PCB 电路板上。

注意：菜单栏提供了 PCB 编辑器的所有菜单文件，只要单击任一主菜单就可得到它的一系列子菜单，利用菜单命令可以完成各项操作。同时，PCB 编辑器也提供了工具栏，它由一系列图标按钮构成，与相应子菜单命令功能相同，亦可通过单击按钮完成相应操作。

3、设置工作参数

（1）环境参数设置：执行菜单命令 Design/Options…，选择“Options”标签，或在设计窗口中单击鼠标右键，选择菜单 Options/Broad Options…。其中

“Grids”栅格设置：

- Snap X、Snap Y ：设定光标每次移动（分别在 X 方向、Y 方向）的最小间距。
- Component X、Component Y：设定移动器件时，光标每次在 X、Y 方向移动的最小间距。
- Visible Kind：设置栅格显示方式，有线状、点状两种方式。

“Electrical Grid”电气栅格设置：Grid Range（格点范围）中设置的数据为半径，以光标所在位置为中心，向四周搜索电气节点。

“Measurement Unit”计量单位设置： 有“Imperial (英制单位)”和“Metric (公制单位)”两种单位。英制单位为“mil（密尔）”，公制单位为“mm(毫米)”。

注意：1mil=0.0254mm。

[技巧]：如果用户已处于 PCB 板设计工作界面，可使用 Ctrl+G 快捷键打开设置 Snap Grids 的编辑对话框来设置。

（2）工作层面设置：选择“Layers”标签，或在设计窗口单击鼠标右键，选择菜单 Options/Broad Layers…，单击 All On 可打开所有工作层面；单击按钮 All Off 可关闭所有工作层面；单击按钮 Used On，可由用户设定工作层面。根据任务要求，双面板需要打开“Signal Layers”项的“Top”和“Bottom”层；元件面上设置丝印层，所以“Silkscreen”项只选择“Top”；两面都要上阻焊漆，所以“Masks”项打开“Top Solder”和“Bottom Solder”；所有元件均采用传统的插针式，不用“Paste Mask”（焊锡膏）。

注意事项：

1、设计双面 PCB 板实际是在一个平面中对两个板层进行设计，必须注意板层切换。

2、信号层和内部板层的添加与删除可以通过板层栈管理器进行，执行菜单命令 Design/Layer Stack Manager…，用户可看到层堆栈的立体效果。

- 单击 Add Layer 按钮可以添加信号层；单击 Add Plane 按钮可添加内层电源/接地层。但在添加信号层前，应该首先使用鼠标单击信号层预添加位置处，然后再设置。
- 选中 Top Dielectric、Bottom Dielectric 复选框，则在顶层、底层添加绝缘层。
- 设置中心层的厚度，则可以在 Core 处编辑设定厚度。

想重新排列中间的信号层，可使用 Move Up 和 Move Down 按钮操作。如果用户需要设置某层的厚度，则可首先选中该层，然后单击 Properties 按钮，进行信号层厚度的设置，还可设置板层名。

3、设计 PCB 板时，系统默认的信号层为两层，机械层默认的只有一层，满足本任务

要求。但是用户可以执行菜单命令 Design/Mechanical Layers…，为 PCB 板设置更多的机械层。

（3）系统参数设置：执行菜单命令 Tools/Preferences…，本次任务无其它特殊参数设置要求，均采用默认设置。

4、自动布局及手工调整

（1）执行菜单命令 Tools/Auto Placement/Auto Placer…。

（2）进入“自动布局”对话框。系统提供了两种自动布局方式：

Cluster Placer：集群布局方式，适合于元件较少的情况，元件被分组放置。

Statistical Placer：统计布局方式，适合于元件较多的情况，元件之间的连线最短，效果好但耗时长，需等待。Statistical Placer 选项如图 8-36 所示，图中各项含义：

- Group Components：将当前网络中连接密切的元件归为一组，元件分组排列。
- Rotate Components：依据当前网络连接与排列的需要，元件可以旋转。
- Power Nets：定义电源网络名称，如 VCC。
- Ground Nets：定义接地网络名称，如 GND。
- Grid Size：设置元件自动布局时的栅格间距，默认值为 20mil。

（3）由于需要设计的 PCB 板中元件较少，根据经验选择“Cluster Placer”布局方式，单击 OK 确定，进入元件自动布局状态，等待几秒钟后自动布局完成。

注意：“飞线”表示元件连接关系，并不是真正的铜膜导线。

（4）手工调整元件布局：

自动布局一般以计算最短布线路径为目标，因此元件的自动布局往往不太理想，需要手工调整元件布局，即对元件进行排列、移动和旋转等操作。

1）元件的排列：执行 Tools／Interactive Placement 子菜单的相关命令，有多种排列方式，其主要命令和功能与模块一原理图编辑器中相同。

2）自动推开元件：执行 Tools／Auto Placement／Set Shove Depth …命令设置推挤次数。执行 Tools／Auto Placement／Shove 命令，光标变成十字，将光标移动到距离很近的元件上，点击鼠标，如果基准元件周围的元件太近，则自动向外推开元件。一般设置 5 次就能满足要求。

3）元件的移动与旋转：用鼠标左键点击需要移动或旋转的元件，并按住左键不放，此时光标变为十字，然后拖动鼠标，则十字光标会带动被选中的元件移动到适当的位置，同时单击键盘的空格键（输入法为英文状态下）使元件以逆时针 90°旋转，最后放开鼠标即可移动或旋转元件到适当位置。

（5）编辑焊盘尺寸：根据实际设计经验，一般封装库中给出的元件焊盘孔径比实际尺寸小，所以必须对 PCB 图中各元件焊盘尺寸重新编辑。一般地， IC 焊盘为 1.6mm x1.8mm（63mil x70mil），插座 1.8 mmx 2.0mm（70 mil x80mil）、一般元件 1.8mm x 1.8mm（70 mil x70mil）。逐一双击元件焊盘，进入该元件焊盘属性对话框进行修改。

5、设置自动布线参数

执行菜单命令 Design/Rules…，单击 Routing 标签，设置自动布线的相关参数，布线规则一般集中在规则类(Rule Classes)中。

（1）Clearance Constraint：设置导线与焊盘之间的安全间距。点击 Clearance Constraint，进入“安全间距设置”对话框，单击下方按钮 Properties…，修改最小安全间距为 15mil。

（2）Routing Corners：设置布线拐角模式。点击 Routing Corners，进入“布线拐角模式设置”对话框，单击下方按钮 Properties…，设置布线拐角为 45º。另外布线拐角还有 90 º和圆脚（Rounded）模式。

（3）Routing Layers：设置布线层及走线方向。点击 Routing Layers，进入“布线层及走线方向”对话框，单击下方按钮 Properties…，其中顶层设置为水平方向布线，底层为垂直方向布线。

（4）Routing Priority：设置布线优先级。点击 Routing Priority，进入“布线优先级设置”对话框，单击下方按钮 Add…，对地线提出优先布线权，设置 GND 网络布线优先级为 1。同样操作设置 VCC 网络布线优先级为 2，其余为 0。

（5）Routing Topology：设置布线模式，即设置焊盘之间的连线方式。对于整个电路板一般选择最短布线模式，但对于电源 VCC 网络、地线 GND 网络，应根据需要选择最短模式（Shortest）、星形模式(Starburst)或菊花链状模式(Daisy-Balanced)，本任务可以使用默认值 Shortest。

（6）Routing Via Style：设置过孔的类型及尺寸。点击 Routing Via Style，进入“过孔的类型设置”对话框，默认过孔尺寸。

（7）Width Constraint：设置布线宽度。点击 Width Constraint，进入“走线宽度”对话框。上述相同操作，增加 VCC 和 GND 网络线宽为 60mil,，修改普通导线线宽为 35mil。

6、自动布线及手工调整

（1）启动自动布线服务器：执行菜单命令 Auto Route / Setup…，在 Routing Passes 设置对话框，定义布线过程中的某些规则。通常，可以采用对话框中的默认设置，自动实现 PCB 板的自动布线，但是如果需要设置某些项，则可以通过对话框的各项操作实现。

（2）自动布线：点击上述操作中 的 Route All 按钮，开始对电路板进行自动布线，完成布线。通过提示框知道：布通率为 100%，布线 29 条，剩余未布导线数为 0，布线时间为 0 秒，单击“OK”按钮即可。

注意：“Auto Route”菜单命令下有五种自动布线方式：

- All：全局布线
- Net：指定网络布线
- Connection：指定两连接点之间布线
- Component：指定元件布线
- Area：指定区域布线

（3）手工调整：虽然 Protel 99 SE 的自动布线成功率几乎高达 100%，但并不代表其布线的结果是合理的。实际上，自动布线的结果往往不能令人满意，最典型的缺点就是布置的走线拐弯太多，有一些布线甚至是舍近求远。因此一个美观、成功的印制电路板往往都需要在自动布线的基础上进行多次手工修改，才能将电路板设计得尽善尽美。手工布线调整实际上就是对布线进行删除、重布、移动等操作。

首先分析需要调整的走线所在层面（如顶层），则将工作层面切换到顶层，作为当前活动的工作层面。然后分别找到起止焊盘位置，分析走线方向，接着执行菜单命令 Place / Interactive Routing，或点击 PlacementTools 工具条上的  按钮，开始布线。走线过程中可能遇到当前工作层面无法布通情况，则通过过孔切换到另一层面（底层）继续布线，最后布线完成之后原来的走线会自动消失。

注意：对于不理想的布线，还可以采用自动拆线方式拆除其中布线，执行菜单命令 Tools/ Un-Route，自动拆线也具有 4 种方式，分别为“All”、“Net”、“Connection”和“Component”，其功能与自动布线相反。

（4）编辑、修改丝印层上元件编号及文字标注：在布局、布线之前，为了便于浏览布局、布线效果，常隐藏元件的编号、型号等信息。将光标指向任一元件，双击鼠标左键打开其元件属性对话框，点击“Global>>”按钮进行全局属性修改，分别将“Designator（编号）”和“Comment（文字标注）”标签中的“Hide 项”选中，点击 OK 后图中所有元件标号和文字标注被隐藏。

注意：1、在丝印层上放置说明性文字，首先必须切换到丝印层（TopOverlay）上，再执行菜单命令 Place/String(放置字符串信息)或点击 PlacementTools 工具条上的  按钮。在丝印层或其它相应工作层上放置说明性文字，操作方法与原理图编辑器中相同。

2、元件编号、型号等信息尽可能靠近该元件的外轮廓线。位于元件面丝印层上的文字标注信息可以放在导线上，但最好不要放在元件轮廓线的边框内，以免元件安装后，元件体本身将文字标注信息遮住；同样文字标注不要放在焊盘或过孔上而无法印上文字信息。

7、设计规则检查：完成 PCB 板设计后，打印前最好利用 Protel 99 SE 提供的检测功能进行规则检测，查看自动布线及手工调整后是否违反了由“Design”菜单下“Rule……”命令所设定的布线规则。

（1）具体操作：执行菜单命令 Tools / Design Rule Check…，“检测选项设置”对话框，提供了两种检测方式：

On-line：在线检测，不产生报告文件，在印刷板编辑区直接给出错误标记。

Report：产生报告文件方式。该方式功能完善，其中“Routing Rules”（布线规则检查项）包括：

■ Clearance Constraint：安全间距。若系统参数设置窗口中允许在线检测，则在自动布线和手工调整过程中，铜膜导线图形间距不会小于设置的安全间距。

- Max/Min Width Constraint：最大/最小线宽限制。
- Short Circuit Constraint：最短走线。
- Un-Route Net Constraint：检查没有布线的网络。

“Manufacturing Rules”（制造规则检查项）：提供了最小夹角、最小焊盘等检查项目。

“High Speed Rules”（高速驱动规则检查项）：提供与高速驱动规则设置有关的检查。

（2）报告文件内容：设置检测选项后，单击按钮 Run DRC，启动设计规则检查，结束后 PCB 编辑器自动进入文本状态，显示检查结果文件“放大整形电路.DRC”。

（3）更正方法：认真分析报告文件中的错误提示信息，回到 PCB 编辑器环境中，单击窗口左侧“Browse“下拉按钮，在列表窗中选择“Violation”（违反规则）项，将“Violation”作为浏览对象。根据错误性质，灵活运用拆线、删除、移动、手工布线以及修改连线属性等编辑手段，修正所有致命错误。然后再运行设计规则检查，直到不出现错误信息，或至少没有致命错误为止。

8、布线后的进一步优化

（1）补泪滴：在电路板设计中，为了让焊盘更坚固，防止机械制板时焊盘与导线断开，常在焊盘和导线之间布置一个过渡区，形状象泪滴，故称做补泪滴。

执行菜单命令 Tool/Teardrops…，默认值是所有的焊盘和过孔补泪滴，泪滴样式有圆弧形（Arc）和导线形（Track）两种。设置完成后单击 OK 即可执行补泪滴操作，效果如图 5-3 所示。

（2）敷铜：为了提高高频电路的抗干扰能力，改善大电流电路中的散热条件，完成布线后，常需要在印刷板的焊锡面、元件面内将关键的网络或大面积空白区域敷满铜膜，一般将所敷的铜膜接地。设置好敷铜属性后，用十字光标去选定敷铜范围的各个端点。

执行菜单命令 Place/Polygon Plane…或单击 PlacementTools 工具条上的 按钮。

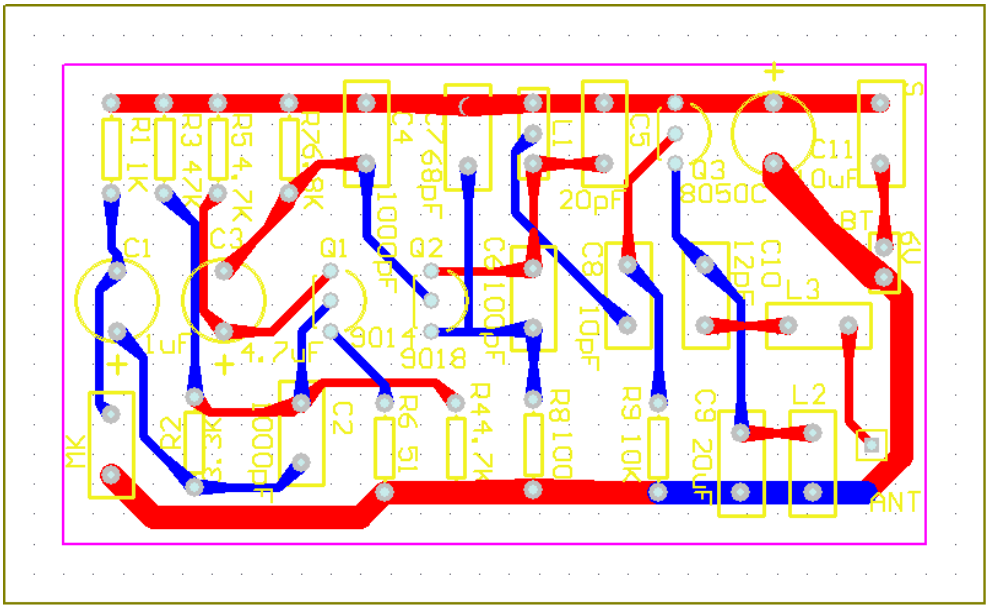


图 5-3

删除敷铜区域方法：执行菜单命令 Edit/Select/Toggle Selection，将光标移到敷铜区域内任意位置，单击鼠标左键选定。再执行菜单命令 Edit/Clear，即可删除已选定的敷铜区域。

（3）包地：高频电路印刷板设计中经常使用包地技术抵抗外界干扰，即将接地的导线包住某一区域或网络。

首先执行菜单命令 Edit/Select/Net，再以十字光标指向所要包地的网络上，鼠标左键确定后即已选择该网络。再执行菜单命令 Tools/Outline Selected Objects，系统自动对被选定的网络进行包地操作，接着撤消选定状态。最后将包地线与地线相连接，即可完成包地操作，效果如图 5-4 所示。

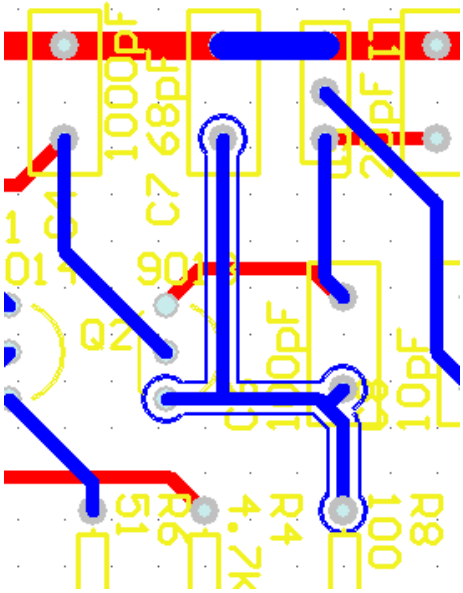


图 5-4

（4）制作螺丝孔：在印刷板四周或板的特殊位置常需要钻螺丝孔，以便于安装与固定电路板，制作螺丝孔可以使用焊盘或过孔来实现，但必须进行额外设置。

首先执行菜单命令 Place/Pad 或单击 PlacementTools 工具条上的按钮，将焊盘分别布置于板四周，然后双击某一焊盘进入其属性对话框，将 X-Size、Y-Size、Hole Size 三项设置为相同值，即均为螺丝孔的直径；在 Advanced 标签中关闭 Plated，确定后板四周的螺丝孔制作完成。

注意：为了使安装孔位置精确，在放置之前最好用菜单命令 Place/Coordinate 或 PlacementTools 工具条上的按钮，在四角上定出孔中心位置坐标，然后再将安装孔放置到指定点上。

（5）3D 效果：3D 效果图可以看出 PCB 的实际效果，从而看到封装是否正确，元件布局是否合理，相互之间是否干涉等问题。

执行菜单命令 View/Board in 3D 或主工具条上的按钮，可以看到 3D 效果。

（6）标注尺寸：出于方便制版过程的考虑，通常需要在 PCB 板上标注某些尺寸的大

小，但尺寸标注不具有电气特性。

步骤一：将当前层面切换到机械层 4（Mechanical4）。

步骤二：执行菜单命令 Place/Dimension 或单击 PlacementTools 工具条上的  按钮。

步骤三：在尺寸标注未放下时，按动键盘上 Tab 键，设置其属性；或者在尺寸标注已放下后，用鼠标左键双击也可设置其属性。在该对话框中可以对尺寸标注的高度（Height）、文字线宽度（Line Width）、单位的显示方式（Unit　Style）、标注文字的高度（Height）、标注文字的宽度（Width）、文字字体（Font）、所在板层（Layer）、起点坐标、终点坐标等进行设置。也可以选择或设定为锁定（Locked）和选择状态（Selected）。

步骤四：将光标移动到合适的位置，然后单击鼠标左键即可放置尺寸标注开始位置，移动光标到结束位置，再次单击鼠标左键即可放置尺寸标注。

9、保存及打印输出

（1）保存电路板设计文件：执行菜单 Files/Save As 命令，在弹出的窗口中选择相应输出文件格式，可生成需要的格式文件。

（2）文件格式转换：执行菜单 Files/Export…命令，在弹出的窗口中选择相应输出文件格式，可生成需要的格式文件。窗口可以将 PCB 文件转换成 AutoCAD 格式文件、HyperLynx 格式文件、PCAD2000 格式文件，这些文件格式都是常用的、流行的格式。

（3）打印输出：先执行 File／Printe／Preview…菜单命令，系统将会生成 Preview 放大整形电路.PPC 文件。进入 Preview 放大整形电路.PPC 文件，然后选择 File／Setup Printer…命令，可以设置打印机的类型。在 Printer 操作框可选择打印机名。在 PCB Filename 编辑框显示了所要打印的文件名。最后执行菜单命令 File／Print 的相关命令进行打印。

实训六

一、 实验/实训内容

1、建立一个新的封装库，取名为“自建 PCB 元件.lib”，包括多个自建的元件封装图；

2、根据图 6-1 电路图直接在 PCB 编辑器中用手动方法设计出实用门铃电路的 PCB 板图，例如图 6-2，其设计要求如下：

（1）单面印刷电路板，手工设计板框尺寸为 2500 mil×1800mil，四角预设安装孔，孔径 120mil。

（2）手工放置元件封装并合理布局。

（3）手工放置铜膜导线，一般铜膜导线宽度 20mil，VCC、GND 网络导线宽度为 50mil。

（4）输出 PCB 报表文件及相关 CAM 文件。

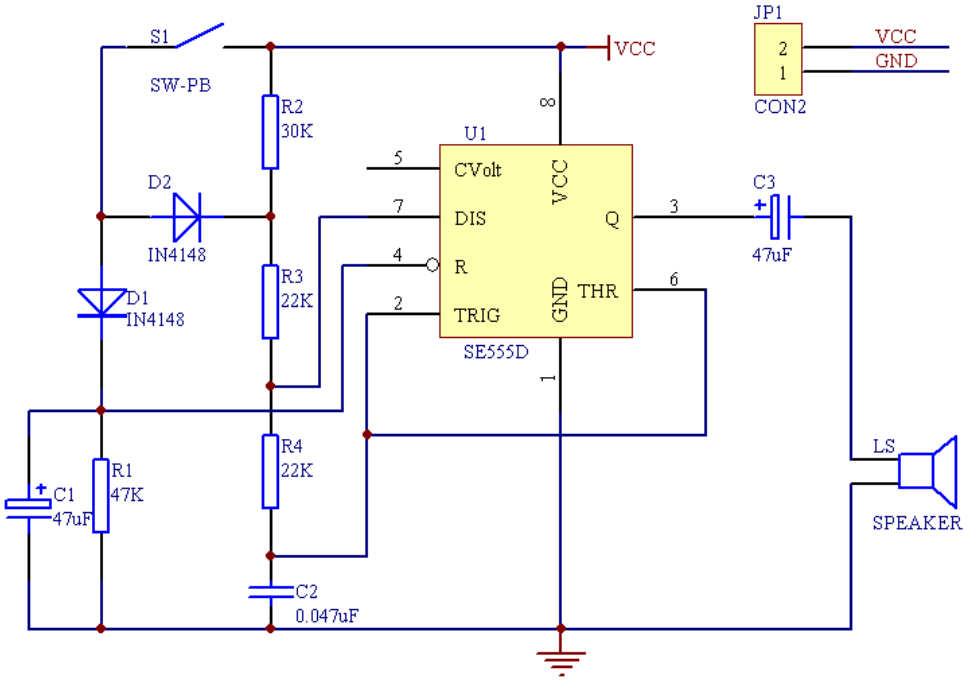


图 6-1

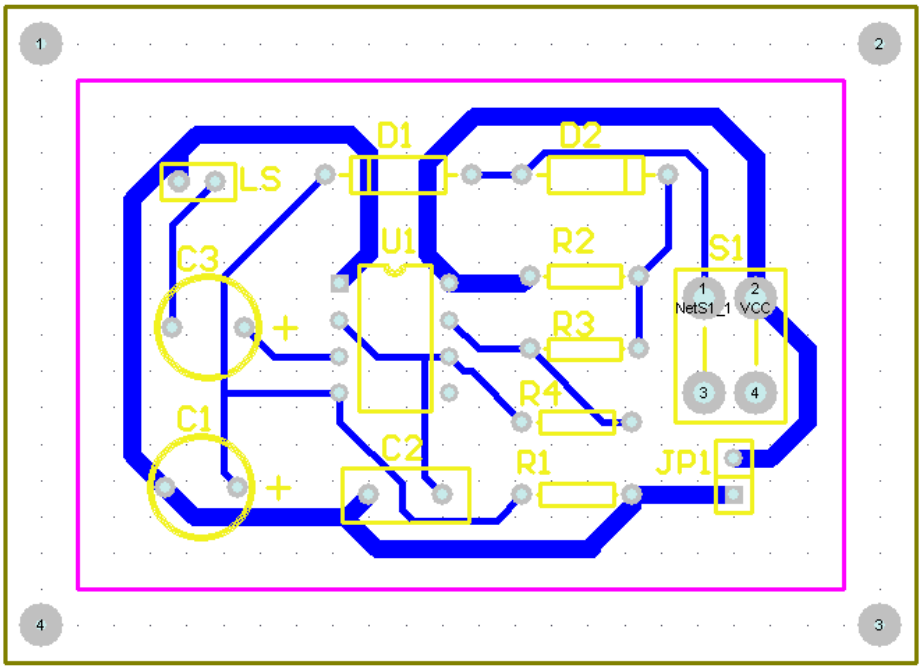


图 6-2

二、 实验/实训要求

1、绘制图 6-1 中需要自创的元件封装。

2、按照实训内容中的技术要求完成单面印制电路板的手动设计。

3、总结本次实训/实验，并撰写实验/实训报告。

三、 实施指导

1、元件封装的编辑与制作：

步骤一：先在当前设计数据库环境下，执行菜单命令 File/New…，进入“New Document”对话框，选择 PCB 元件库编辑器图标。双击该图标或单击 OK 按钮后，系统在当前设计数据库中建立一个新元件封装库文件，修改文件名为“自建 PCB 元件.lib”。然后双击该文件图标，进入 PCB 封装库编辑器工作界面。

步骤二：设置 PCB 封装库编辑器环境

（1）编辑区调整。最初进入 PCB 封装库的编辑区内有一个十字坐标轴，其中心坐标为原点（0，0）。单击鼠标右键，选择 Library Options…命令， Layers 标签中打开第一可视栅格，关闭第二可视栅格；Options 标签中将定位栅格均设置为 5mil，电气栅格取 4mil。

（2）工作参数及图纸参数设置。执行菜单命令 Tools/Preferences…，可以对工作层、焊盘、过孔等的显示颜色、光标形状等信息设置。

（3）打开封装库管理器。点击 View/Design Manager，选择 Browse PCBLib 标签，可切换到封装库管理器。其中 Components(元件列表）窗口内容与原理图元件库编辑器相同，Update PCB 按钮功能是更新 PCB 图中有关该元件的信息，即在元件封装库编辑器中所做的修改可相应反应到电路板中。

步骤三：手工创建元件封装，利用绘图工具完成。在实用门铃电路.ddb 中新建 PCB 封

装库文件“自建封装.LIB”，在库中分别自建 C1、C3 电解电容封装图和 S1 按钮封装图。

步骤四：向导创建元件封装，按照向导提示完成。

2、新建 PCB 文件

在实用门铃电路数据库(实用门铃电路.ddb)的 Documents 界面，执行菜单命令 File / New…，或单击鼠标右键选择 New…命令，选择“PCB Document”，建立“实用门铃电路.PCB”文件。

3、设置工作参数：

（1）环境参数设置：执行菜单命令 Design/Options…，选择“Options”标签，或在设计窗口中单击鼠标右键，选择菜单 Options/Broad Options…。为使定位更精确，将 X、Y 方向定位栅格设置为 10mil，其他均为默认设置。

（2）系统参数设置：执行菜单命令 Tools/Preferences…，无特殊要求各项则采用默认值。

4、规划电路板

（1）添加机械层：机械层没有电气特性，Protel 99 SE 一般只需使用 1～2 个机械层，主要用于定义电路板的物理边框、标注 PCB 板关键部位尺寸及电路板生产过程中的对准孔。

执行菜单命令 Design/Mechanical Layers…，添加 Mechanical 1、Mechanical 4 机械层。

（2）单面板工作层面设置：

执行菜单命令 Design/ Layer Stack Manager…，单击左下脚的 Menu 按钮，在弹出的菜单中选择 Example Layer Stacks/Single Layer，此时顶层变为元件面，底层变为焊接面。

执行菜单命令 Design/Options…，或在设计窗口单击鼠标右键，选择菜单 Options/Broad Layers…，选择“Layers”标签，由于设计是单面板，同时还要有丝印层、底层阻焊膜层、禁止层和穿透层，布线只在焊接面进行。

（3）手工定义电路板形状及尺寸：分别在机械层 4 和禁止布线层绘制出电路板的物理边界和电气边界。

KeepOutLayer （禁止布线层）是 PCB 工作空间中一个用来确定有效放置元件和布线区域的特殊工作层面。电气边界就是通过在 KeepOutLayer 层上绘制边界来限定布局和布线的范围。用鼠标单击编辑区下方的 

标签，将当前工作层面切换到 KeepOutLayer，步骤如下：

步骤 1：执行菜单命令 Place/Line，或单击放置工具栏中的  按钮，此时光标变成十字状。

步骤 2：移动光标到编辑区（0，0）点，单击鼠标左键，即可确定第一条边的起点。然后拖动鼠标，将光标移动到（2500，0）点，单击鼠标左键，即可确定第一条边的终点。

步骤 3：依次用同样方法绘制其它 3 条板边，坐标点分别为（2500，0）、（2500，1800）、（0，1800），单击鼠标右键，退出画线命令状态。至此，绘制出一个 2500mil×1800mil 的

封闭矩形边框，

步骤 4：双击画线可进入 Track 属性对话框，可精确地进行定位，并且可以设置工作层面和线宽。

同样物理边界在 Mechanical4 (机械 4 层)上绘制，其规划与上述电气边界方法完全相同，本例中两边界间距 200mil。

注意：

1、通常情况下，应将电气边界与物理边界范围规划成相同大小，但为了放置螺丝孔，本任务设计中的电气边界及物理边界的间隔 200mil。

2、若开始时没有确切的电路板尺寸，可以先画一个框，待布线完成后再重新按上述方法定义电路板边框尺寸。边框线距离元件引脚焊盘最小距离必须大于 2mm，否则下料比较困难。

（4）预设安装孔：电路板的 4 个角上放置 4 个安装孔，以便于安装。

5、装入元件封装库

（1）加载自建元件封装库：调用实用门铃电路.ddb 中新建 PCB 封装库文件“自建封装.LIB”。

（2）加载元件封装库：执行菜单命令 Design/Add/Remove Library…，或单击窗口左侧的“Browse PCB”按钮，在下拉选项中选择“Library”，点击 Add/Remove….按钮，装入 “自建封装.lib”库文件。

6、手动布局

（1）放置、编辑元件封装：先确定电路中核心元件或对位置有特殊要求的元件位置。首先放置时基电路集成块 SE555D，其次放置外围元件。

执行菜单命令 Place/Component…，或点击 PlacementTools 工具条上的  按钮，进入，输入元件封装、编号及元件类型等信息，而后单击“OK”按钮即可调出 U1（DIP8），在编辑区合适位置单击鼠标左键即可放置该元件，同时将再次输入下一个元件的封装、标号和注释内容。放置完成后，单击对话框中的“Cancel”按钮，或者按下 Esc 键，取消放置元件命令状态。

注意：

1、在元件未放下时按动 Tab 键，可设置元件属性，如图 11-18 所示，封装和编号不能省略，出于保密可以隐藏注释信息。

2、电源和地不需放置元件，有相应连接器连接。

技巧：执行菜单命令 Edit/Origin/Set，将光标移至电路板布局区域内单击鼠标左键，即可设置相对原点。目的是：当布局区域不在当前可视编辑区内时，按动快捷键 Ctrl + End 可使布局区域显示在当前屏幕上。

（2）手动布局：通过平移、旋转等操作方式调整元件及其编号的位置，同时必须遵循元件布局的相关原则，具体操作方法参见任务八中有关手工调整元件布局相关内容。反复调

整后的布局效果如图 11-19 所示。

注意：手动布局不可能一次成功，在后面的布线过程中还将反复进行操作，以便更方便、合理地走线。

7、手动布线

由于各元件封装是逐个放置的，并未加载网络表，所以各元件之间是独立的，从图 11-19 中可以看出，各个元件之间没有预拉线，它们之间的连接需要对照图 11-1 实用门铃电路原理图手动放置铜膜导线来完成。

（1）选择布线层：单面板只能在 BottomLayer 层（焊锡面 Solder Side）布线，故将工作层面切换到 Solder Side 面。

技巧：通过小键盘上的 * 或 + 键选择当前板层， * 键只能在顶层和底层间切换。

（2）设置布线参数：执行菜单命令 Design/Rules…，单击 Routing 标签，选择 Routing Corners，设置布线拐角为 45º 。

选择 Routing Layers，设置布线层面，关闭 Component Side，仅在 Solder Side 布线。

选择 Width Constraint，设置普通铜膜走线宽度为 20mil。

（3）放置铜膜导线：执行菜单命令 Place／Interactive Routing，或点击 PlacementTools 工具条上的  按钮，光标变成十字，移动光标到起点（一般为焊盘），单击鼠标左键确定，继续移动光标可以看到一条活动的连接线。当光标移动到导线转折处，单击鼠标左键确定，直到终点焊盘处，再次单击鼠标左键确定，单击鼠标右键终止连线，即可绘制出一条铜膜导线。此时仍处于连线状态，可以继续放置其他铜膜导线。当需要取消连线操作时，再次单击鼠标右键或按下 Esc 键返回。

注意：（1）根据任务要求需要 VCC 和接地导线线宽为 50mil，在连接 VCC 或接地导线过程中，注意线宽应设置成 50mil。

（2）手工布线需要认真、细致、反复地操作，甚至布线过程中为了更合理方便走线，还需要回到前面步骤，重新手动调整布局，再重新布线。

8、PCB 报表输出

（1）引脚信息报表：该报表能够将电路板上被选取的引脚的相关信息提供给用户，并建立扩展名为.dmp 的引脚信息报表文件，让用户较方便地检验网络上的连线。

步骤 1：切换工作层面到元件面（即 TopLayer），在电路板上选取需要生成报表的引脚。

步骤 2：执行菜单命令 Reports/Selected Pins…， “选取引脚（Select Pins）信息”对话框，列出了被选取的引脚信息。

步骤 3：点击 OK 按钮，进入“实用门铃电路.DMP”引脚报表文件。

（2）电路板信息报表：该报表给用户提供了一个电路板的完整信息，包括电路板尺寸、电路板上的焊盘、导孔的数量、导线数量以及电路板上的零件标号等信息内容。

步骤 1：执行菜单命令 Reports/Board Information…，进入“电路板信息”对话框。其中：

General 选项卡：显示电路板的一般信息，包括电路板尺寸、电路板上各个组件的数量，

如导线数、焊盘数、导孔数、敷铜数、违反设计规则的数量等。

Components 选项卡：显示当前电路板上使用的零件序号以及零件所在的板层等信息。

Nets 选项卡：显示当前电路板中的网络总数和网络列表。

步骤 2：在任何选项卡中点击 Report 按钮，得到“选项报表项目”对话框。根据需要选择产生报表的项目，Selected Objects 复选框只产生选中对象的电路板信息报表。

步骤 3：点击 Report 按钮，生成相应的“实用门铃电路.REP”电路板信息报表文件。

（3）其他相关输出：菜单 Report 下还有其他报告如下：

Design Hierarchy：输出设计的层面报告。

Netlist Status：输出网络状态报表。

Measure Distance：测量任意两点间的距离。

Measure Primitives：测量电路板上焊盘、连线和导孔间的距离。

9、CAM 文件的输出

电路板设计完成后，习惯将 PCB 电路板文件直接送入电路板工厂进行加工制作，而实际上出于技术保密、准确等方面的原因，最好将由 Protel 99 SE 创建的辅助制作电路板文件，即 CAM（Computer Aid Manufacture ）文件送入加工厂，其中光绘（Gerber）文件和 NC 钻孔文件是最重要的 PCB 生产文件。

（1）元件报表：该报表用于整理电路中的零件，形成一个元件列表。在大型电路板设计工作中，元件报表为后期元件采购工作带来极大便利。生成元件报表的操作步骤如下：

步骤 1：执行菜单命令 File／CAM Manager…，进入 CAM 文件向导。

步骤 2：单击 Next 按钮，选择 BOM(Bill of Material)类型。

步骤 3：单击 Next 按钮，输入 BOM 名称为：实用门铃电路。

步骤 4：单击 Next 按钮，选择 BOM 报表格式，Spreadsheet 为 Excel 表格式；Text 为文本格式；CSV 为字符串形式。

步骤 5：单击 Next 按钮，选择元件的列表形式，系统提供了两种列表形式：

- List：将当前电路板上所有元件列表，每一个元件占一行，所有元件按顺序向下排列。
- Group：将当前电路板上具有相同元件封装值和元件名称的元件作为一组，每组占一行。

步骤 6：单击 Next 按钮，选择 Comment，用元件名称来对元件报表排序，并选择元件报表范围，包括 Designator、Footprint 和 Comment。

步骤 7：单击 Next 按钮，单击 Finish 按钮，即可产生辅助制造管理器文件，即“CAM Outputs for 实用门铃电路.cam”文件，本文件中创建了一个“实用门铃电路.Bom”报表，但此时还不能查看到报表的内容。

步骤 8：在 CAM Outputs for 实用门铃电路.cam 文件中，执行菜单命令 Tools/Generate CAM Files，系统将产生 BOM for 实用门铃电路.Bom 等元件报表文件，打开 BOM for 实用门铃电路.Bom 文件，元件报表（以 Excel 表格显示）。

（2）NC 钻孔文件：钻孔文件提供了制作电路板时所需的钻孔资料，可直接用于数控

钻孔机，生成 NC 钻孔文件操作步骤如下：

步骤 1：在 CAM Outputs for 实用门铃电路.cam 文件中，执行菜单命令 Tools/CAM Wizard…,，选择 NC Drill 类型。

步骤 2：单击 Next 按钮，输入 NC Drill 文件名为：实用门铃电路。

步骤 3：单击 Next 按钮，选择英制或公制单位，并选择单位格式（其中 2:3 格式单位的分辨率为 1mil，2:4 格式单位的分辨率为 0.1mil，2:5 格式单位的分辨率为 0.01mil）。

步骤 4：单击 Next 按钮，最后弹出结束对话框，单击 Finish 按钮后，在 CAM Outputs for 实用门铃电路.cam 文件中又创建了“实用门铃电路.NC Drill”文件，此时还不能看到钻孔文件的内容，用上述同样的方法可以看到钻孔信息。

（3）光绘文件：光绘文件是 Gerber Scientific 公司开发的用于驱动光学绘图仪的底片文件格式，作用在于为生产厂家在加工制作印制电路板时提供详细的制作资料，使生产出的电路板真正符合设计者的要求。生成光绘文件的步骤如下：

步骤 1：在 CAM Outputs for 实用门铃电路.cam 文件中，执行菜单命令 Tools/CAM Wizard…,选择 Gerber 类型。然后单击 Next 按钮。

步骤 2：单击 Next 按钮，输入 Gerber 文件名为实用门铃电路。

步骤 3：单击 Next 按钮，说明生成的文件格式是自动配置孔径文件的 RS274X。

步骤 4：单击 Next 按钮，选择测量单位和分辨率。

步骤 5：单击 Next 按钮，选择输出的图层和是否需要镜像翻转。

步骤 6：单击 Next 按钮，询问是否生成钻孔图和钻孔指导图。

步骤 7：单击 Next 按钮，询问是否设置钻孔图中的层对、钻孔图符号类型、字符、钻孔字符串、尺寸和是否镜像。

步骤 8：单击 Next 按钮，询问是否设置钻孔指导图中的层对和是否镜像。

步骤 9：单击 Next 按钮，询问是否将机械层的内容加到 Gerber 文件中。

步骤 10：单击 Finish 按钮，即可创建了“实用门铃电路.Gerber”文件。同样按照上述方法，系统将产生实用门铃电路的 13 份文件，切换到 CAM for 实用门铃电路文件夹，可以看到本实例的光绘文件。

词汇表（部分）

Schematic document
Electrical
Grid
Miscellaneous device
Bjt
Crystal
Diode
Simulation
Resistor
Capacity
Wire
Line
Bus
Bus entry
Net label
Port
Junction
Sheet symbol
Sheet entry
Annotation
Transient
Simulate
PLD
Place
Reports
Tools
Design
View
Edit
Save
Export
Import
Paste
Jump
Zoom in
Zoom out
Netlist
Preference
Run
Setup
Complie
Bill of material
Electro
Fuse
Inductor
Jfet
Mosfet
Nand
Nor
Not
Npn
Pnp
Buffer
BJT
OPAmp
Relay
Teardrop
AC
DC
ERC
Design
Create netlist
Footprint
Designator
Part
Layer
Mechanical
Drilldrawing
Multilayer
Arcs
String
Pad
Via
Silkscreen
Mask
Polygon
Placement
Route
CAM